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A GaN-Based Synchronous Rectifier with Reduced Voltage Distortion for 6.78 MHz Wireless Power Applications

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To the Graduate Council:

I am submitting herewith a thesis written by Spencer Pierce Cochran entitled "A GaN-Based Synchronous Rectifier with Reduced Voltage Distortion for 6.78 MHz Wireless Power Applications." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

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A GaN-Based Synchronous Rectifier with Reduced Voltage Distortion for 6.78 MHz Wireless Power Applications

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As is true of all I do, this Master's Thesis is dedicated to my savior and friend,

Jesus, the one through whom all else finds meaning.

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"Education without values, as useful as it is, seems rather to make man a more clever devil."

- C. S. Lewis

Abstract

The call for a larger degree of engineering innovation grows as wireless power transfer increases in popularity. In this thesis, 6.78 MHz resonant wireless power transfer is explained. Challenges in WPT such as dynamic load variation and electromagnetic interference due to harmonic distortion are discussed, and a literature review is conducted to convey how the current state of the art is addressing these challenges.

A GaN-based synchronous rectifier is proposed as a viable solution, and a model of the circuit is constructed. The precisely derived model is compared to a linearized model to illustrate the importance of exactness within the model derivation. The model is then used to quantify the design space of circuit parameters L_r and C_r with regard to harmonic distortion, input phase control, and efficiency. Practical design decisions concerning the 6.78 MHz system are explained. These include gate driver choice and mitigation of PCB parasitics. The model is verified with open loop experimentation using a linear power amplifier, FPGA, electronic load, and two function generators. Current zero-crossing sensing is then introduced in order to achieve self-regulation of both the switching frequency and input phase. The details

of the FPGA code and sensing scheme used to obtain this closed loop functionality are described in detail. Finally, conclusions are drawn, and future work is identified.

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Chapter 1

Introduction

Wireless power transfer (WPT) can be separated into "high" and "low" power categories. High power applications are generally related to the charging of electric vehicles. The power levels of these systems are typically greater than one kilowatt [4]. Low power applications are generally focused on consumer devices (i.e. cell phones, tables, laptops, wearables, etc.). Sub-watt implantable WPT medical technology also exists, but this thesis will be focused on consumer device applications. The power levels of WPT systems for these devices is in the 1 to 10's of watts range.

1.1 Inductive Power Transfer Overview

Consumer devices have proven methods of charging, yet wireless power transfer continues to grow as a technology. A few things push WPT forward in the market. First, there is always a "wow" factor with new technology, especially if that technology

is easy to use and difficult to understand. This draws in early adopters and promotes new technological innovation. Furthermore, wireless power helps to meet practical consumer needs. Seamless wireless charging increases ease of use and provides a means to improve charging safety, by removing both the hassle and potential failure of charging cables. Future WPT could improve immunity to liquids, chemicals, and dirt, and WPT could potentially even reduce battery sizes by making charging a more frequent and public endeavor [5, 6]. Due to factors like these, the market for WPT technology is projected to be worth greater than 13 billion USD by the year 2020 [7].

Basic inductive power transfer (IPT) systems have been available to the public for the last 6+ years [5]. The basic principle of operation for an inductively coupled charging system is that of a transformer. A basic transformer uses core material and electrically conductive windings to magnetically couple two (or more) circuits. This results in the transfer of energy between two points that have no mutual electrical connection. Inductive power transfer uses the same principles. A primary coil is placed in a grid-connected circuit to supply power, and a receiver coil is placed in a device-connected circuit to receive power. When the two coils are in close proximity they magnetically couple, employing air (and anything else in between them) as their mutual core material. Like a transformer, electrical power is transferred from supply to device in the absence of any electrical connection. Figure 1.1 shows how the physical WPT system translates to transformer in a circuit.

Powermat launched inductively coupled charging technology in 2009. In Japan, members of the Power Mater Alliance (PMA) soon followed with launches of their

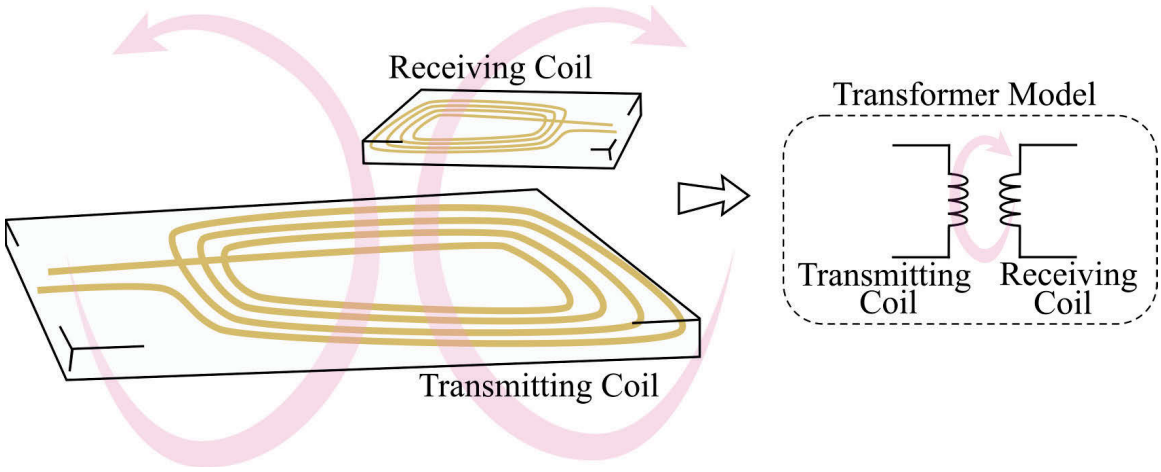


Figure 1.1: Illustration of how WPT magnetic coupling translates to a transformer model.

own in 2011 [5]. Qi (pronounced "chee") is the leading international standard for inductively coupled charging. The Qi method utilizes tightly coupled coils to transfer power over a distance of millimeters [6, 8]. For inductively coupled systems, coil alignment is crucial for power transfer. System efficiency drops off rapidly as coil coupling factor decreases. Furthermore, current commercial Qi charging is generally thought of as a single-device procedure (i.e. only one device charges at a time) [5]. However, employing a coil array in the transmission pad allows for both increased on-pad orientation freedom and multi-device charging [8].

Low-power Qi operates at 5 W and in the frequency range of 110 - 205 kHz. Powers up to 120 W are supported by the medium-power Qi standard which operates in the frequency range of 80 - 300 kHz. One distinct advantage of tightly coupled IPT system is its ability to support in-band communications. The Qi standard maintains this advantage, allowing device and charger to send and receive digital signals via the same magnetic coupling used for power transfer [5, 6, 8].

IPT works under a "tightly coupled" charging mechanism. This accounts for the protocol's innate sensitivity to coil alignment, coil spacial orientation, and charging distance. Inductive power transfer is most commonly used between two flat surfaces. For example, a flat transmission pad charges a flat receiving device (such as a cell phone). Wearable technology, bluetooth earpieces, and any other device shape that could interfere with a flush transmitter-receiver alignment makes IPT difficult to implement [5].

1.2 Magnetic Resonance

A WPT set-up wherein the sending and receiving circuitry are tuned to have a resonance at the fundamental operating frequency is called a "magnetic resonance" system. As the magnetic resonance standard was being developed by the Alliance for Wireless Power (A4WP), the term "LC WPT" was used due to describe the technique [9]. This terminology is explanatory because the combination of inductance and capacitance is what allows a designer to tune WPT circuitry to a specific resonant frequency. For the receiver, generally the inductance used to tune the circuit is the receiving coil (also called the "secondary," much like a transformer). A capacitor is added to make the receiver appropriately resonant at the operating frequency.

Resonance is not a new concept in its own regard, but it becomes a powerful ally when applied to WPT. Magnetic resonant WPT systems are built to be loosely coupled. Loose coupling is the result of a less intense magnetic field passing

through the receiver coil. The resonance of the system and system-wide increase in fundamental frequency both enable evanescent-wave coupling, a characteristic that permits WPT to take place even when the coils are loosely coupled [8]. Evanescent-wave coupling allows high efficiency energy transfer between resonant components, while the system loses very little to non-resonant externalities [8]. The ability to operate with a smaller magnetic coupling results in more spacial orientation, coil design, coil alignment, and multi-coupling freedoms [5]. Figure 1.2 illustrates some basic differences between tight coupling and loose resonant coupling.

These advantages are some of the reasons that the A4WP saw fit to develope a WPT standard that competes with the Qi standard. The predominant standard used in research and development of magnetic resonance technology is called "Rezence" [6]. It should be noted that, recently, AirFuel has taken over for A4WP and converted the Rezence standard to the AirFuel Resonant standard. However, this thesis was written using Rezence documentation and will be referencing the Rezence standard throughout the remainder of the discussion.

The Rezence standard uses a "power transmission unit" (PTU) to supply a "power receiving unit" (PRU). For clarity, using "PTU and PRU" terminology is similar to referencing "sender and receiver" or "primary and secondary" circuitry. The charging distance between PTU and PRU can be upwards of a few meters, removing the necessity of flush spacial orientation as in IPT [6, 8]. The fundamental operating frequency of the Rezence standard is 6.78 MHz, which is a significant increase from

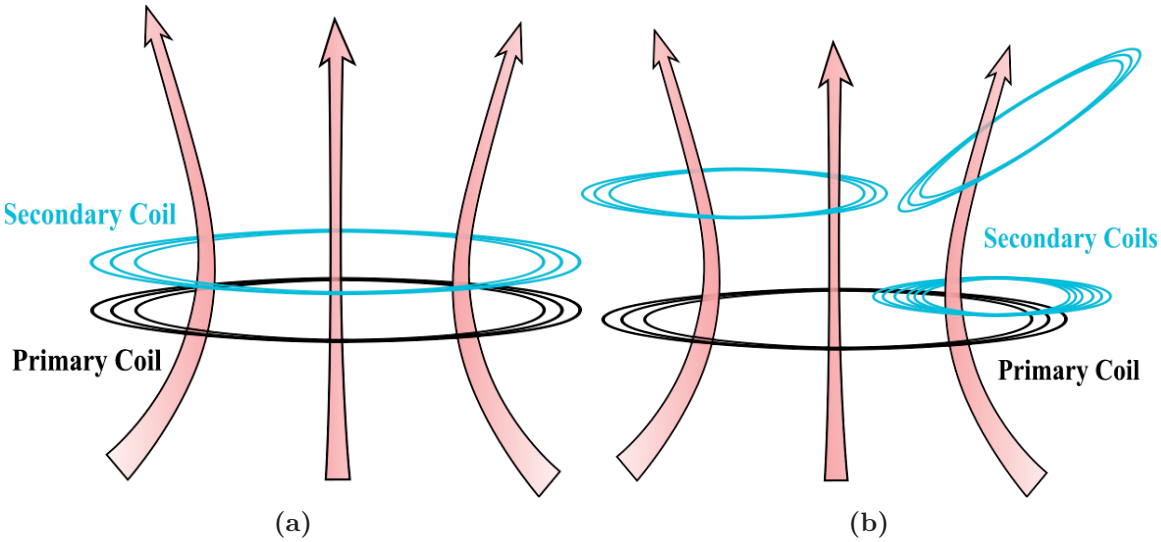


Figure 1.2: Comparison of a (a) tightly coupled IPT system and (b) loosely coupled magnetic resonance system.

the Qi protocol. The increase in operating frequency helps to answer the call for longer charging distances and smaller circuits [10, 11]

The standard allows for a single PTU to charge multiple PRUs, each at a different power level. It also names different PTU classes (highest class has 70 W input power) and requires that the PTU be able to charge a minimum of n (depending on the PTU class) devices in parallel [12]. Rezence uses Bluetooth Low Energy (BLE) to send communications between PTU and PRU. This is generally considered a disadvantage when compared with the in-band communications of the IPT Qi systems [5, 12].

1.3 WPT System

Magnetic resonance will be the genre of WPT referenced throughout the remainder of this thesis. Figure 1.3 shows a typical single-PRU wireless power

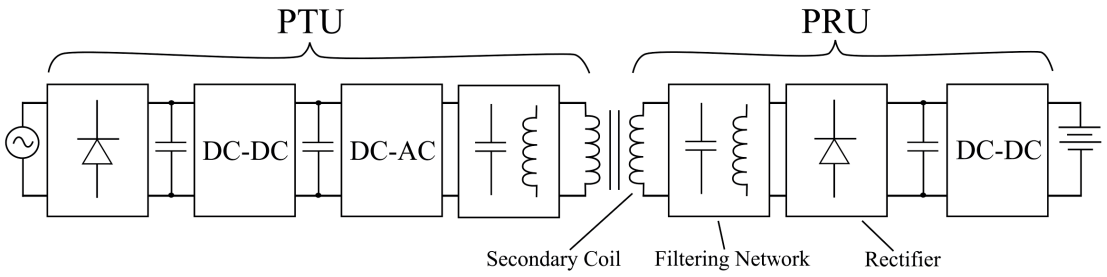


Figure 1.3: Wireless power transfer system overview.

transfer system layout. A general power transmitting unit consists of a rectifier, a DC-DC converter, a DC-AC converter, and some filtering to complement the operating frequency. These stages conclude with the transmission coil which is matched with capacitance, creating the resonance necessary to properly utilize a loosely coupled link.

The PRU consists of the secondary (receiving) coil, a filtering network, and a rectifier. Finally some sort of load regulation (a DC-DC converter is shown here) is connected between the rectifier and the battery to be charged. It is important to note that there are numerous topologies for implementing a WPT system, and Figure 1.3 is not comprehensive but acts as an example.

This work will be focused on secondary circuitry for WPT systems. More specifically, the discussion will be centered around the secondary coil, matching network, and rectifier stages. However, seeing as the proposed circuit composes only the rectifier stage, this thesis does not include models of either the secondary coil or the filtering network as named in Figure 1.3. Therefore, while both of these elements will be important parts of the discussion, steps will be taken to abstract away from any actual coil or filter design in this thesis.

1.4 Summary

Wireless power transfer works by coupling the magnetic fields of two electrically isolated inductive coils. An inductive power transfer system uses tight coupling at 100's of kHz to transfer power. Limitations include restricted charging distance, orientation, and single receiver charged by a transmitter. A resonant power transfer system utilizes loose coupling at around 10 MHz to transfer power. This system is limited by lack of in-band communications but sees an increase in charging distance, flexibility of orientation, and simultaneous charge capability.

This section is followed by a literature review, during which the largest challenges will be explained. Shortcomings of techniques previously used at lower frequencies will be pointed out, and the current trends of consumer-device WPT PRU rectification will be discussed. Gallium nitride (GaN) will be introduced as a good candidate for multi-megahertz applications, and a GaN-based rectifier will be proposed to address the field of Rezence-based research from a new perspective.

The literature review is found in Chapter 2. In Chapter 3, the circuit is explained, modeled, and simulated. The design criteria explains how a designer navigates certain trade-offs of the topology from a high-level system point of view. Following this, Chapter 4 delves into the closed loop experimental model verification and includes a discussion of how parasitic PCB inductance is mitigated via improved layout. Chapter 5 contains the sensing schemes and the experimental setup used for closed loop testing. Finally, Chapter 6 provides a summary, draws conclusions, and discusses

the future work that needs to be considered in order to continue refining the modeling and control of proposed rectifier.

Chapter 2

Literature Review

The market for wireless power pushes the technological development of more user-friendly systems. The call for higher power, longer charging distance, and smaller circuitry has driven the operating frequency of WPT systems into the megahertz range [10, 11]. The most competitive standard for consumer-device WPT, Rezence, operates at 6.78 MHz. In contrast to the IPT techniques which commonly operate in the 100's of kilohertz range, a multi-megahertz frequency presents various challenges. These challenges include the relevance of parasitic content, the obvious increase in switching loss, and the attenuation strategy for high frequency harmonic content.

2.1 Coil Harmonic Content

Recall that in Figure 1.3 the primary and secondary coils are enclosed by filtering stages. Harmonic content on the transmitting and receiving coils will create

unwanted electromagnetic interference (EMI). EMI is potentially intrusive to other nearby devices, and EMI can cause difficulty in meeting regulations related to the industrial, scientific, and medical (ISM) operating frequency band [1, 13]. One simple design approach to prevent a circuit from radiating too much EMI is to shield the coils. However, the coils in a WPT system cannot be shielded because doing so would block the system's magnetic coupling, rendering wireless power transfer impossible. It is therefore imperative that harmonic content is attenuated near the primary and secondary coils, and the filtering stages in Figure 1.3 are placed to accomplish this.

The problem with filtering is that it takes up valuable circuit board space, a commodity that grows more scarce as consumer devices shrink. A signal that contains large amounts of harmonic content requires larger amounts of filtering, which costs space. Furthermore, each element in a filter contains non-idealities, and consequently, filters with many stages incur a larger amount of loss. For these reasons, multi-stage filtering stages are generally unattractive to WPT systems.

Consider a simplified ideal diode rectifier that is driven by a sinusoidal input current. This rectifier will have waveforms as seen in Figure 2.1. The voltage at the input of the rectifier is a square wave, a wave shape that contains harmonic content out to infinite frequencies. If a secondary coil connected where the current source is illustrated, the coil would be subject to large amounts of high frequency harmonic content via the applied voltage waveform. Again, to fix the ensuing EMI issues, a designer might add a multi-stage filter. This example simply illustrates that the filtering stages are often "band-aids" meant to patch problems that arise elsewhere.

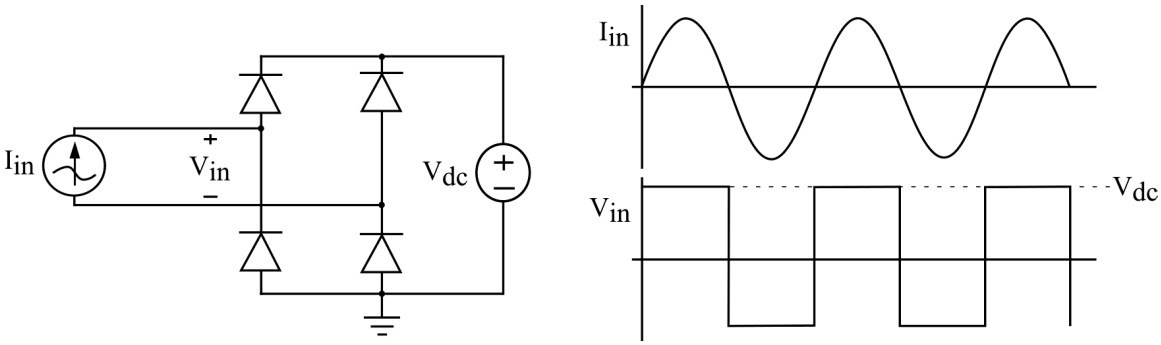


Figure 2.1: Ideal current-driven diode rectifier and input waveforms.

In the case of the secondary side, the harmonic content is created by the rectifier. A more novel approach is to rectify in such a way that it either mitigates or removes the need for filtering. Generally speaking, lowering the harmonic content created by the process of rectification reduces both the size and loss of a multi-stage filter.

Class E topologies are being widely studied for use in WPT systems, both in transmission-side designs [14, 15, 16, 17] and receiving-side designs [1, 11, 14, 16, 18, 19, 20, 21]. The class E inverter, first introduced in [22], is commonly considered a good fit for high frequency WPT applications due to its simple construction and megahertz zero-voltage switching (ZVS) capability [15, 16, 22]. The same work that initially introduced class E rectification also gives an example of the topology's high frequency application, building and testing a model that works at 22 MHz. It also reports that the class E rectifier can utilize parasitics in actual design [23]. Using parasitics is especially attractive at higher frequencies.

At the secondary side, class E rectifiers have another advantage that complements WPT applications. Class E rectification has nearly sinusoidal input waveforms [23]. This means that class E rectifiers have low total harmonic distortion (THD) at the

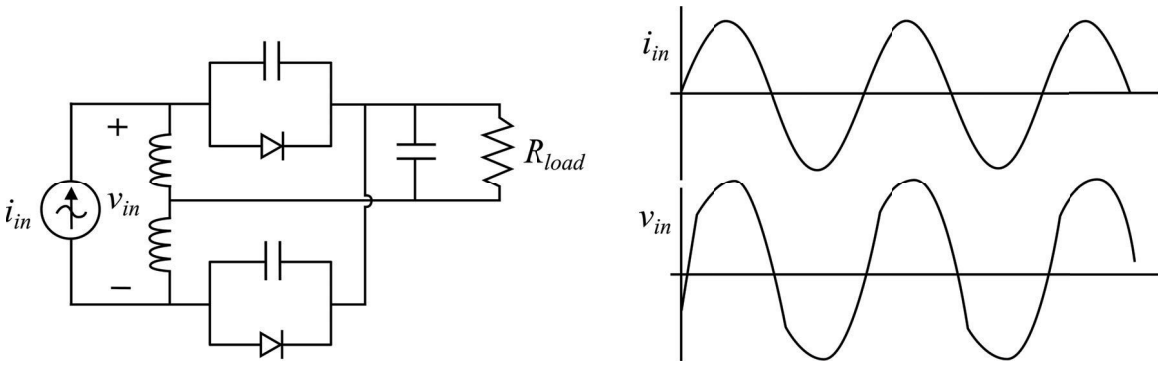


Figure 2.2: Example current driven class E full-wave lowdv/dt rectifier circuit and waveforms adapted from [1].

input. More specifically, class E rectifiers can be split into lowdv/dt and lowdi/dt categories, where each type focuses on the implementation of ZVS and ZCS (zero current switching), respectively [24]. In contrast to the V_{in} waveform in Figure 2.1, an input voltage waveform with low THD results in less required filtering for the secondary coil. Therefore, class E rectifiers are good candidates for reducing the need for filtering. An example class E full-wave rectifier and its corresponding waveforms can be seen in Figure 2.2.

With these considerations for high frequency WPT systems, it follows that research of class E rectifiers for WPT topics is prolific. At 800 kHz, a piecewise linear state space model is used to evaluate the performance of class E rectification at the secondary side [19]. The ensuing experiments see the rectifier hooked to the IPT transmitter in [25] and demonstrate a 10 W system with peak rectifier efficiency of 94.43% [19]. Work set at 6.78 MHz considers the input impedance to a class E rectifier as an important variable in assuring the secondary coil is tuned at frequency [11]. A genetics algorithm is applied to improve the "robustness" of the WPT system

when considering varying loading conditions, resulting in higher efficiencies as load and coupling change [11]. Paper [1] compares a class E rectifier and a traditional full-bridge rectifier at 6.78 MHz in terms of THD, efficiency, power factor, and voltage/current transfer functions. As previously discussed, [1] highlights the class E rectifier's significant decrease in THD (by a factor of four) in the comparison. Other examples of class E rectification at 6.78 MHz show an individual rectifier efficiency of greater than 91% and a WPT system efficiency of greater than 83% [20, 21].

Using both a class E PA and class E rectifier, a system-wide optimization is conducted by minimizing average power loss across loading conditions during the battery charging process. The study elaborates on those systems optimized for a single operating point [14]. In a later work, "class E^2" is used to describe the DC-DC converter created by joining a class E PA, a WPT magnetic resonant link, and a class E rectifier [16]. The work in [16] discusses the same system "robustness" as [11] and proposes both methodology and design technique to improve stability and efficiency with varying coil alignment and load condition [16].

The advantages of class E topologies have been discussed, but factors other than input voltage THD and ZVS must be considered in order to find a good overall approach to WPT rectification. Efficiency is one such factor. The ZVS techniques used in class E rectification can be extended to other rectifier topologies, making other topologies competitive for this application. Futhermore, dynamic control is beneficial for multi-load systems, and as WPT systems grow in complexity, a solution that adds system-wide control may be beneficial [26].

2.2 Impedance Matching

In a WPT system, the ability to change spacial orientation/distance (coupling factor), number of simultaneous PRUs, and the respective powers of each PRU ultimately results in a large field of primary side loading conditions. The methods by which researchers are exploring solutions for dynamic loading are discussed here. Such a large set of loading possibilities can potentially contain regions of extremely low efficiency operation, or by poor design, areas wherein the primary side inverter cannot safely supply power. This problem can be addressed by impedance matching. The process of developing strategies for impedance matching is another challenge that WPT designers face when working on megahertz magnetic resonant systems.

There is a significant amount of research concerning how to handle the issues that arise with multiple receivers [26, 27, 28, 29, 30]. Varying a single receiver's coupling coefficient and DC load can dramatically change efficiency [11]. To make matters more complex, when multiple receivers are coupled to a single transmission coil, the receiver coils have a tendency to couple to one another as well. It has been shown that this "cross coupling" decreases efficiency in multi-charging WPT systems [27]. It is possible to account for the effects of cross coupling via dynamic control of the secondary reactance. The work in [26] addresses the issue of cross coupling and concludes that "the decrease in the system efficiency due to the nonzero cross coupling can largely be recovered by having the optimal load reactances." An application of dynamic control might be increasing the system-wide efficiency via

optimization of operational trajectory and/or compensation of the negative effects of cross coupling.

One method for compensating the reactive portion of the primary side equivalent load is through the use of an adaptive impedance matching network (IMN) at the transmitter. Changing the value of a circuit capacitance is generally done by switching among various capacitors so that the equivalent capacitance is optimized. This is called a "π-match network" or a "switching capacitor bank" [29, 31, 32]. One work in particular focuses on varying the compensation capacitance in the secondary side instead of the primary side [15]. This method is simulated and shown to improve system efficiency by significantly correcting unwanted load angle due to various coil alignments and parasitics [33]. An IPT compensation method using a saturable DC-feed inductor (varying inductance instead of capacitance) in a class E inverter is proposed in [15].

Some methods for improving the effects of cross coupling and various loading conditions do not involve real-time impedance matching. These techniques are mostly of improved design procedure [11, 16, 30]. One example uses capacitive impedance matching networks at both the transmitter and receiver [30]. The two types of IMNs are called series-parallel (SP) and parallel-series (PS). The IMNs in this study have designed values of capacitance and contain no switching functionality, emphasizing the differences between the SP and PS structures. Using a SP IMN at the receiver makes the transfer efficiency of each device less sensitive to variation in the load. In contrast, using a PS IMN at the receiver yields better system immunity to

cross coupling [30]. Once again concerning static design improvement, two papers related to WPT "robustness" are addressing the system efficiency for a wide range of loading conditions by improving overall design methodology [11, 16]. The system is considered more "robust" as the total average efficiency is increased across all loading conditions [11, 16].

All of these methods have some level of corresponding drawback, however. Capacitor banks require large amounts of unused board space, as many capacitors are left idle for each operating point. The DC-feed inductor incurs extra loss (up to 0.911 W maximum in a $\sim$12 W system) and size [15]. The design solutions offer a system improvement in terms of robustness and/or stability. However, they solve the problem in a limited manner, wherein the overall average efficiency trend is improved but no dynamic circuit response is available for addressing real time misalignment or cross coupling. The difference between performing design optimization for a static system across a load range and allowing a dynamic system to self-optimize for each individual operating point across the same load range should be pointed out.

Another method to achieve impedance matching is done by utilizing the unique properties of a synchronous rectifier. Synchronous full-bridge rectification allows the designer control over the rectifier input phase. Furthermore, by means of either special rectifier switch modulation scheme or a DC-DC converter between the rectifier and the battery, the system shown in [34, 35] is able to control the magnitude of the secondary side equivalent impedance. The switching rectifier can be directed to switch at any time during the period, and in doing so, the phase relationship between input

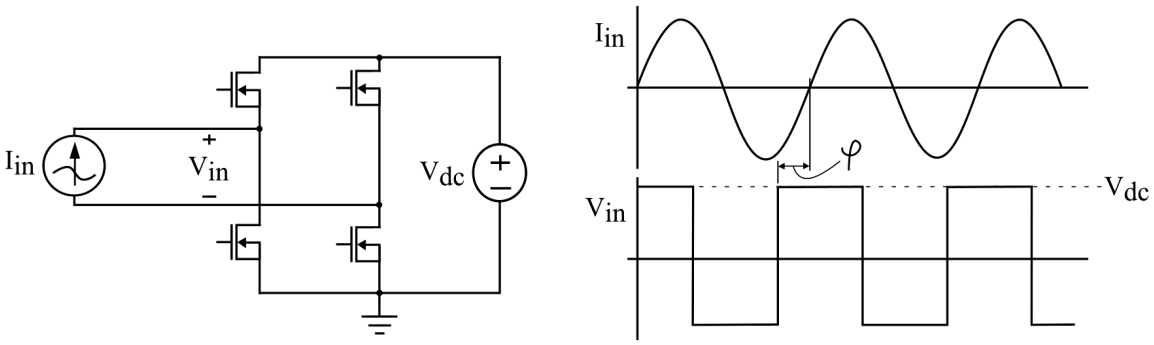


Figure 2.3: Ideal current-driven switching rectifier and input waveforms.

voltage and current can be controlled. The magnitude of secondary impedance can be controlled by means of duty cycle. The important takeaway for this technique is that power factor correction (equivalent impedance reactive component manipulation) can be done via synchronous rectification for a wide loading range [34, 35].

Figure 2.3 gives a rudimentary example of what the waveforms of a synchronous full-bridge rectifier look like. The variable φ denotes the phase at the input of the rectifier. φ is controlled via the rectifier switching signals. This makes things like matching the load impedance to the complex conjugate of the transmitter impedance possible. This matching is the point of maximum power transfer because it makes the reactive portion of the equivalent load impedance zero [36]. However, if given a specific WPT system design, this real-time variability enables the rectifier to tune itself to whichever point is more optimal for the system, even if that point is not the complex conjugate of the transmitter impedance.

The 6.78 MHz switching frequency employed by the Rezence standard makes large switching losses difficult to entertain. The synchronous work in [34, 35] is for the IPT

Qi standard operating in the 100's of kilohertz range. As noted by [37], the main trade-off for synchronous rectifiers is switching loss, and in transitioning from 100 kHz to 6.78 MHz, switching loss increases by over one order of magnitude. Although the conduction loss in a switching full-bridge is less than that of a diode full-bridge, the increase in switching loss often overpowers the losses saved by this lower conduction loss. Therefore, soft-switching techniques make synchronous rectification a better candidate at 6.78 MHz because they eliminate the majority of the synchronous rectifier's switching loss.

2.3 Gallium Nitride (GaN)

Enhancement mode gallium nitride (eGaN) devices were introduced by Efficient Power Conversion Corporation (EPC) for power applications in 2009 [38]. At a fundamental level, GaNFETs behave similarly to MOSFETs. EPC boasts that, for certain applications, GaN works at higher switching frequencies, efficiencies, and power densities when compared with silicon (Si) MOSFETs [39]. As a point of comparison, EPC shows a figure of merit (FOM) used to compare devices in terms of on-state resistance (R_{DS}) and gate charge (Q_g) in Figure 2.4 [39]. Note that the devices shown in Figure 2.4 are below 200 V, and the devices used in this research fall into that range. These FOMs will lead to lower gate switching losses for applications with similar conduction losses.

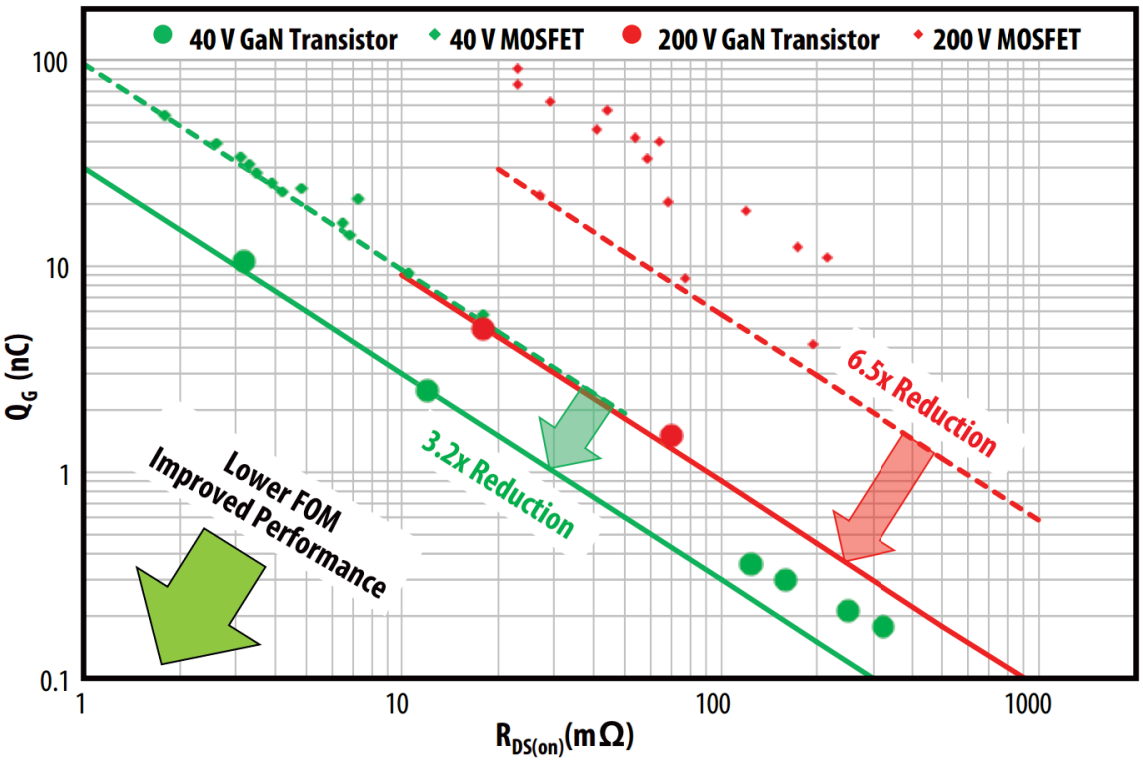


Figure 2.4: FOM reduction of EPC GaNFETs vs traditional devices [2].

A few significant differences between GaNFETs and MOSFETs are worth noting. First, GaNFETs do not have a traditional body diode. Reverse conduction in the source-to-drain direction is possible with GaN, but the reverse conduction mechanism tends to take place near 2 V [40]. This leads to higher reverse conduction losses if no external diode is used. Reverse conduction takes place when the gate-to-drain voltage reaches its threshold and turns the device on. The threshold voltage ($\tilde{2}$ V) remains across the device, causing relatively high reverse conduction losses. However, the reverse conduction process does not include minority carriers, and for this reason, GaNFETs do not exhibit reverse recovery charge. Next, the gate has a lower turn-on threshold voltage, at around 1.5 V, and a lower gate maximum over-voltage tolerance, rated at around 6 V [41]. The allowable driving voltage window is consequently much smaller than a conventional MOSFET, allowing little room for error due to ringing or control fault.

Due to GaN's relatively new presence in the field of power electronics, many papers include discussion and/or research on topics like device characteristics and device driving schemes [2, 38, 39, 40, 41, 42, 43]. For driving a half-bridge, the LM5113 gate driver from Texas Instruments is a popular choice [41, 42, 44]. In particular, [41] discusses many important factors in using GaN for high frequency switching applications. Things like separate gate sourcing and sinking paths, optimal design PCB layout (minimizing parasitics), and consideration of gate drive supply voltage are discussed and compared using two converters: one optimized and the

other non-optimized. A greater than 2% efficiency increase is seen in the optimized converter (800 kHz, 100 V GaN devices) [41].

Furthermore, a fair amount of work is being done with GaN devices switching in the megahertz frequency range [10, 42, 44, 45, 46]. A step-down converter from 42-53 V to 12 V at the output switches at 5 MHz and has a maximum output power of 120 W [44]. In [45], a 20 W LED light bulb is driven by a GaN-based circuit utilizing switching frequencies between 2.5 and 4.4 MHz. A study conducted at 6.78 MHz WPT contains a GaN-based inverter, a Schottky diode rectifier, and a 500 kHz buck converter. The DC to DC efficiency is recorded at 73% [46].

Most notably, a GaN-based synchronous rectifier is applied to a wireless power transfer system in [10]. In this design, the low-side GaN gate nodes are tied to the high-side GaN sources. Recalling the GaN maximum over-voltage tolerance of 6 V, this topology essentially limits the rectifier output voltage to 5 V because during on-state conduction the output voltage is equal to low-side V_{GS} [41]. Nevertheless, the 6.78 MHz system showcases a 3 A, 15 W maximum output power and a 91.8% maximum efficiency with under 1 W of total power loss at full power [10].

Due to the advantages discussed in this section, this work aims to utilize gallium nitride to address issues surrounding magnetic resonance WPT at 6.78 MHz. A portion of the discussion will contain findings regarding optimal GaN layout, gate drive choice/scheme, and best practice.

2.4 Summary and Motivation

Wireless power transfer has moved up in switching frequency with the growing popularity of magnetic resonance techniques. 6.78 MHz operation and loosely coupled Rezence systems are promising for expanding the potential of the state of the art. However, the ever-growing possibilities of WPT are married to new engineering challenges.

EMI radiating from the unshielded coils of a WPT system is often difficult to control. A multi-stage filter may solve the problems of passive full-bridge rectification, but it does so at the cost of size and efficiency. Class E rectifiers have characteristics that make them good candidates for compensating for this issue, and a significant amount of research has been presented for this type of WPT rectification. However, class E topologies may not be the most holistic answer for addressing all significant issues connected to the secondary-side of a WPT system.

Power factor correction becomes drastically more important when considering the wide range of loading conditions available to WPT systems under the Rezence standard. The cross coupling effect of multi-receiver architectures is one such mechanism that reduces system efficiency. Solutions to these loading issues are generally either bulky or static average improvements. The techniques used by switching rectifiers present an elegant solution for complex conjugate matching, but implementation at 6.78 MHz is difficult due to device switching time and device

switching loss. ZVS techniques will be highly beneficial for any switching full-bridge operating at the frequency of the Rezence standard.

Gallium nitride FETs are relatively new to power electronics research. However, for lower voltage applications (as in this application), GaN devices still present significant advantage in terms of switching loss, switching frequency, and power density. Current GaN research includes device characterization and optimization of layout principles. Multiple GaN-based power electronics systems demonstrate successful operation in the multi-megahertz range. Overall, Gallium Nitride FET technology serves to enable switching at 6.78 MHz via its increased switching speed and lower gate capacitance.

Chapter 3

Modeling and Design

The work in this thesis is focused on a GaN-based synchronous rectifier for 6.78 MHz WPT applications. The topology proposed here is able to achieve ZVS, therefore drastically reducing circuit losses. The ZVS transitions are intentionally "slowed" to improve THD and mitigate the need for harmonic filtering. And it is shown that, by correct design, it is possible to include the resonant tank while maintaining the ability to control the rectifier's input impedance for purposes of dynamic load angle correction in a WPT system. The topology proposed in this thesis addresses the issues outlined in the literature review: THD, impedance matching, and switching loss (magnified at high frequencies).

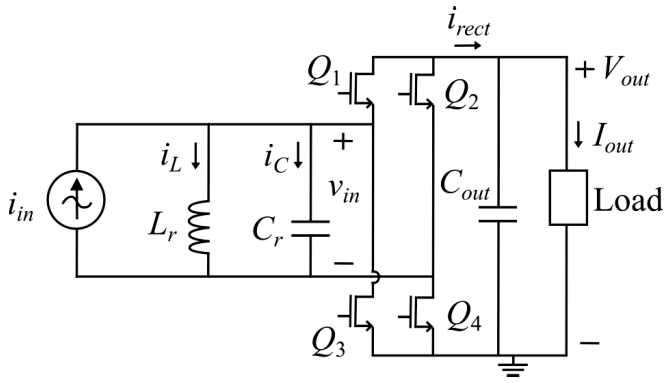


Figure 3.1: Proposed synchronous, current-driven rectifier.

3.1 Fundamental Operation

The advantages of this topology address the challenges presented in Chapter 2. Namely, this circuit gives design control over the THD of v_{in} via an elegant ZVS transition, and the equivalent input phase of the rectifier is controllable via switch timing. However, there are notable design tradeoffs within the system. For example, the level of THD robustness with respect to input phase change is related to resonant tank losses and circulating current. To further explore these types of tradeoffs within the design process, an understanding of how the circuit is modeled must first be established.

The proposed synchronous rectifier uses switching actions to achieve rectification of the input signal. Figure 3.1 shows the basic circuit topology. The input current of the rectifier is modeled as an ideal sinusoidal source. The elements L_r and C_r are resonant tank elements. Switches Q_{1-4} are GaN devices that switch at the system's fundamental frequency, 6.78 MHz. C_{out} is considered to be a large filter element, and consequently, V_{out} is modeled as a DC value.

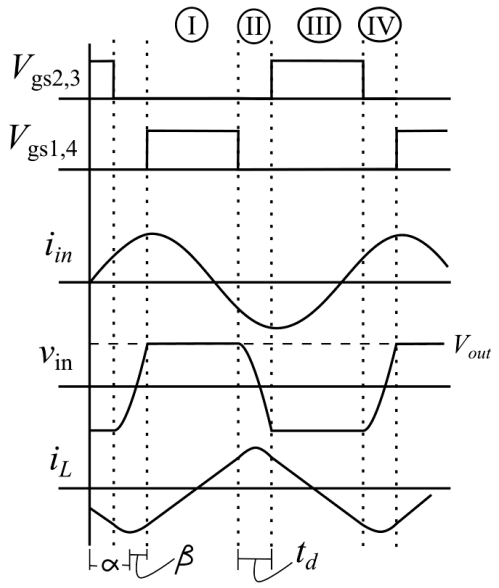


Figure 3.2: Example waveforms of the proposed circuit.

Like a diode full bridge, the majority of the power is delivered to the load when either Q_1 and Q_4 or Q_2 and Q_3 are conducting. These are intervals I and III on Figure 3.2. During these power delivery intervals, the input voltage, v_{in}, is equal to the DC output voltage, V_{out}, and the input current is directed to the load through the filtering capacitor C_{out}. The equivalent circuit for this stage can be seen in Figure 3.3a. The time during which all switches are open is the dead time, t_d. The resonant tank elements, L_r and C_r, facilitate a ZVS operation such that v_{in} transitions from $\pm V_{out}$ to $\mp V_{out}$. The equivalent circuit during the dead time is shown in Figure 3.3b.

The tank inductor current, i_L, undergoes linear rise or fall during power delivery because L_r is biased by $\pm V_{out}$. During the dead time, the current in L_r resonates with C_r as shown in Figure 3.2. This resonance is biased by the sinusoidal input current source, as seen in Figure 3.3b.

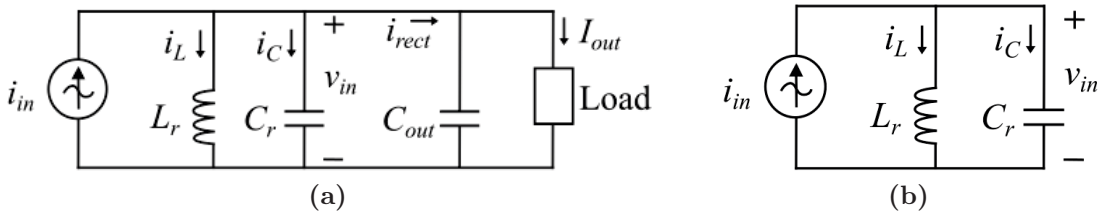


Figure 3.3: Equivalent circuits during (a) the conduction of switches Q_1 and Q_4 (quadrant I) and (b) the dead time (quadrants II and IV).

The rectifier's equivalent input phase is controlled by changing the switching times relative to the input current. The variable that relates the center of the dead time to the zero crossing of i_{in} is α, as shown in Figure 3.2. The variable β is equivalent to one-half of the dead time in radians. Therefore, the beginning and end of the dead time for any operating point are written as $\alpha + \beta$ and $\alpha - \beta$ respectively.

3.2 Dead Time Modeling

The equivalent dead time resonance circuit is shown in Figure 3.3b. The resonance between L_r and C_r includes the input current. Equation (3.1) is the KCL of the dead time circuit of Figure 3.3b, and it shows how i_C is dependent on i_L as well as i_{in}.

$$i_{\text{C\_dt}} = i_{\text{in\_dt}} - i_{\text{L\_dt}} \tag{3.1}$$

Because input phase control is regulated via the variable α, the section of i_{in} exposed to the resonant transition changes with input phase. Therefore, depending on the variable α, the value of i_{in_dt} during the dead time is different. In Figure 3.4, the

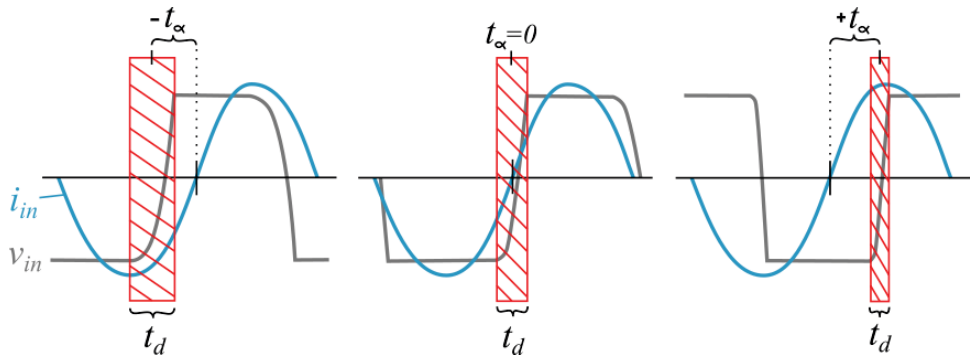


Figure 3.4: Illustration of how v_{in}, i_{in}, and t_d change with α. Negative, zero, and positive α values are shown here respectively.

variable t_α is defined as

$$t_\alpha = \alpha/\omega_s \tag{3.2}$$

where $\omega_s = 2\pi(6.78 \text{ MHz})$. When α is negative, the input current is opposite the inductor current, reducing the net current flowing into C_r during the dead time. With reduced i_{C_dt}, the dead time is increased in order to retain ZVS. This dynamic is illustrated in Figure 3.4. The opposite effect is shown for positive values of α. Current i_{in_dt} complements current i_{L_dt}, and the total current flowing into C_r is increased. With increased i_{C_dt}, the dead time is shorter because v_{in} transitions from $\pm V_{out}$ to $\mp V_{out}$ more quickly.

The presence of a sinusoidal i_{in} during the dead time makes the mathematical derivation of the dead time resonance significantly more difficult. Modeling techniques like state plane analysis are used to model LC resonances with DC bias. In this way, 2_{nd} order linear differential equations are modeled with trigonometric methods. Here however, the practical usability of something like state plane analysis is undercut by the time variance of i_{in}. Equations (3.3) and (3.4) are the KCL and KVL equations

for the dead time circuit as shown in Figure 3.3b.

$$i_{\text{in\_dt}} = i_{\text{L\_dt}} + C_{\text{r}} \frac{dv_{\text{C\_dt}}}{dt} \tag{3.3}$$

$$v_{\text{C}} = L_{\text{r}} \frac{di_{\text{L\_dt}}}{dt} \tag{3.4}$$

Combining (3.3) and (3.4) results in equation (3.5) below.

$$i_{\text{in\_dt}} \frac{1}{L_{\text{r}} C_{\text{r}}} = \frac{1}{L_{\text{r}} C_{\text{r}}} i_{\text{L\_dt}}(t) + \frac{d^2 i_{\text{L\_dt}}}{dt^2} \tag{3.5}$$

Here, i_{in_dt} is a section of a sinusoid represented by (3.6).

$$i_{\text{in\_td}}(t) = I_{\text{in}} \sin\left(\omega_s \left(t + \frac{\beta - \alpha}{\omega_{\text{s}}}\right)\right) \tag{3.6}$$

The variable I_{in} is the peak value of i_{in}. Plugging (3.6) into (3.5) creates a 2^{nd} order linear non-homogeneous differential equation. Solving this equation gives i_{L_td} as a function of time, t. This solution is shown in (3.7) where I_1 is the initial inductor current at the beginning of the dead time and ω_t is the resonant frequency of the tank in radians.

$$\begin{aligned} i_{L\_td}(t) = {} & I_1 \cos\left(\omega_t \left(t + \frac{\beta - \alpha}{\omega_s}\right)\right) + C_r V_{out} \omega_t \sin\left(\omega_t \left(t + \frac{\beta - \alpha}{\omega_s}\right)\right) + \\ & \frac{I_{in}}{\left(\frac{\omega_s^2}{\omega_t^2} - 1\right)} \left[\cos\left(\omega_t \left(t + \frac{\beta - \alpha}{\omega_s}\right)\right) \sin(\alpha - \beta) + \right. \\ & \left. \frac{\omega_s}{\omega_t} \sin\left(\omega_t \left(t + \frac{\beta - \alpha}{\omega_s}\right)\right) \cos(\alpha - \beta) + \sin(\omega_s t) \right] \end{aligned} \tag{3.7}$$

The dead time circuit waveforms of Figure 3.3b can be solved by iteration of (3.3) and (3.4) with a small time step. This is the derivation strategy for a circuit simulation program like LTspice. An advantage of this method is its accuracy in depicting transient conditions. However, a significant drawback is that simulation takes a long time, and it is therefore difficult to sweep different circuit parameters because the circuit must be changed manually between each iteration of simulation. Equation (3.7) is implemented into a MATLAB code, and is used to solve for circuit waveforms during the dead time. Practically, (3.7) enables a relatively quick sweep of variables like β, α, L_r, C_r, and V_{out}. The code model enables a high-level design view of circuit waveforms, design trade-offs, and operation dependencies of the aforementioned variables.

3.3 Code Model

Equation (3.7) is the cornerstone of the circuit model. Given the dead time and I_1, the value of i_L at the end of the dead time can be calculated via equation (3.7). The variable I_1 is defined as the initial value of i_L during the dead time (interval II). The value of I_1 is not known, so I_1 is swept inside the code model, calculating i_L at the end of the dead time in each case. This value is defined as I_2. After this, the linear change in i_L due to interval III is calculated with

$$i_{\mathrm{L}}(t) = I_2 + \Big(t - \frac{(\alpha+\beta)}{\omega_s}\Big)\Big(\frac{-V_{\mathrm{out}}}{L}\Big). \tag{3.8}$$

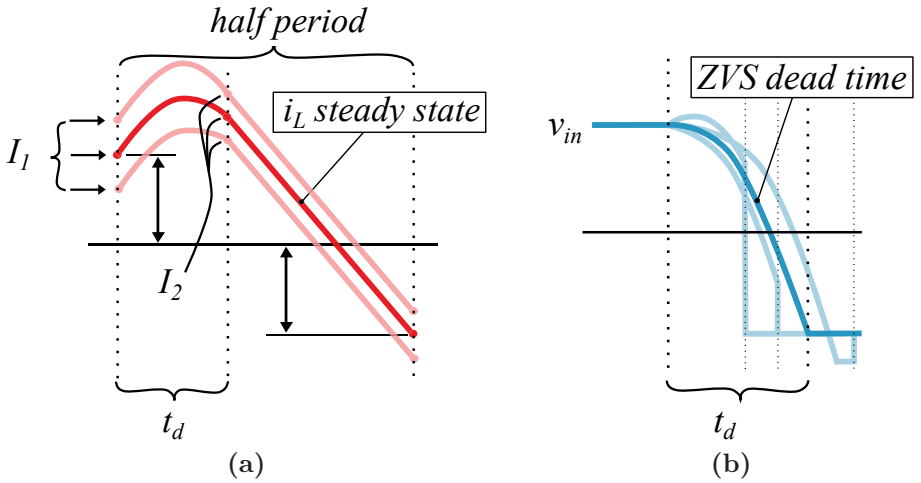


Figure 3.5: Processes for (a) finding the steady state operating point and (b) find the optimal dead time for ZVS.

The final value of i_L for the half period is compared with I_1 to find the steady state operating point. This process is outlined by Figure 3.5a. The steady state i_L is found given the dead time, but the dead time is not known and therefore must be swept as well. A ZVS criterion is added for the choice of dead time. Given the steady state i_L waveform, the i_{C_dt} waveform can also be constructed. This enables derivation of the v_{in_dt} waveform, and the ZVS criterion is then employed to choose the optimal dead time. This process is shown in Figure 3.5b.

This method gives the steady state operating point and optimal dead time for a given V_{out}, I_{in}, L_r, C_r, and α. The waveforms of i_C and v_{in} can be precisely calculated. Figure 3.6 shows example simulated circuit waveforms for a given V_{out}, I_{in}, L_r, and C_r. The variable α is swept, and the process explained by Figure 3.5 is used for each value of α. By visual inspection of Figure 3.6 one can see that the currents i_{in} and

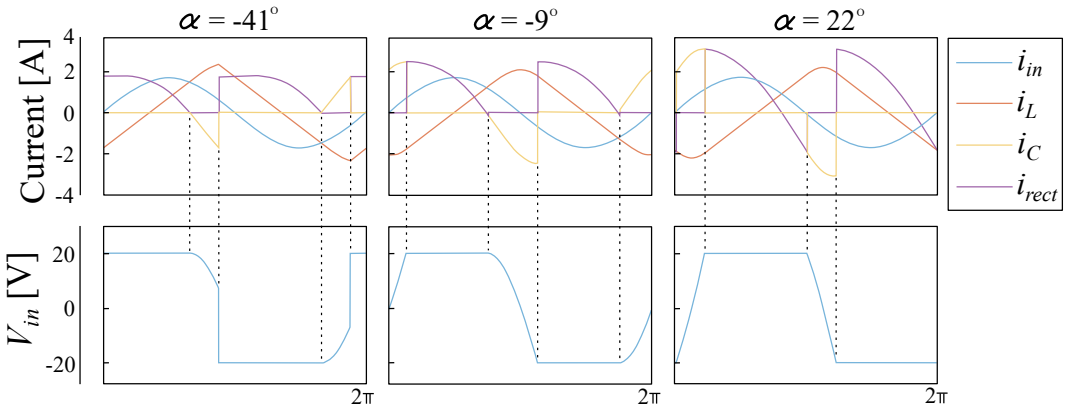


Figure 3.6: Example circuit simulation waveforms found by sweeping α while keeping V_{out}, L_r, and C_r constant.

$-i_L$ sum to i_C as dictated by (3.1). Furthermore, one can see that the dead time is optimized to achieve ZVS when possible.

These waveforms can then be used to calculate things like THD, efficiency, and a number of other useful parameters. This modeling method gives insight into circuit operation. In this work, THD is derived using

$$THD\ [\%] = 100 * \frac{\sqrt{v_{in\_RMS}^2 - v_{fund\_RMS}^2}}{v_{fund\_RMS}^2} \tag{3.9}$$

where v_{in_RMS} is the RMS voltage of v_{in}, and v_{fund_RMS} is the RMS value of the fundamental component of v_{in}.

Figure 3.7 shows graphs wherein each data point is derived from a set of generated waveforms like the three examples shown in Figure 3.6. The results in Figure 3.7 are the output of a simulation holding L_r, C_r, and i_{in} constant while sweeping the variables V_{out} and α. Sweeping these two variables allows for the data to be filtered such that the output power is constant. The results in Figure 3.7 are for a constant

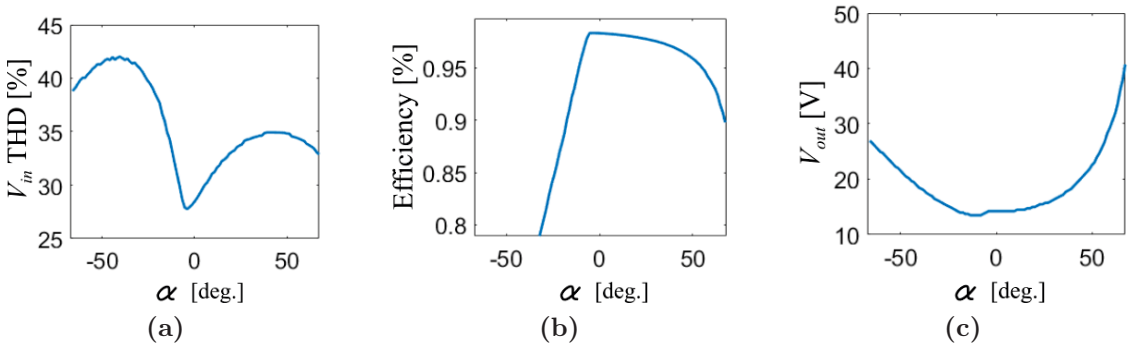


Figure 3.7: Example simulation results found by sweeping V_{out} and α while keeping L_r, C_r, I_{in}, and P_{out} constant. The constant values are $L_r = 300$ nH, $C_r = 1050$ pF, $I_{in} = 1.75$ A, and $P_{out} = 15$ W. The graphed results are (a) the THD of v_{in}, (b) the system efficiency, and (c) the output voltage, V_{out}.

15 W output power. The characteristics shown are the THD of v_{in} (Figure 3.7a), the system efficiency (Figure 3.7b), and the output voltage (Figure 3.7c) for each value of α. Figure 3.7 provides an example of how the model is able to illustrate the relationships between circuit parameters like THD and α.

The valley near $\alpha \approx -10^o$ in Figure 3.7a is the α at which the circuit is first able to achieve ZVS. Circuits with values of α below this threshold incur hard switching losses, and circuits with values larger (up to $\alpha = 90^o$) are able to achieve ZVS. However, conduction losses increase as alpha increases, meaning that the value of α where ZVS is first attained is also the peak efficiency of the system. Due to the presence of i_{in}, negative values of α make ZVS more difficult to attain, and positive values of α make ZVS easier to obtain. This dynamic is due to the mechanism demonstrated in Figure 3.4 and is discussed in the previous section. Essentially, Figure 3.7b shows that values of α that incur hard switching also showcase low efficiency values and

high values of THD, confirming that the desired operation region is within the ZVS range.

The precise derivation of the dead time resonance in equation (3.7) and the inclusion thereof into the code infrastructure prove to be valuable components of the system model. This modeling system returns precise results, as will be demonstrated in the next section when the model is compared to a linearized model. The modeling system also returns timely results, something that can not be said of solving for each parameter by hand calculations. The combination of precision and timeliness enables the model to characterize the design space of L_r and C_r.

3.4 Model Comparison

In previous work, a piecewise linear model is used to characterize the behavior of the proposed circuit [47]. The piecewise model approximates the dead time with a straight line, the slope of which is calculated using both i_{in} and i_L. In this section, the two models are compared in order to validate the proposed modeling method, wherein the dead time is precisely derived by equation (3.7). In [47] the dead time is fixed, and both hard switching and diode conduction are allowed. Here, the piecewise linear model is constructed using dynamic ZVS dead times in order to establish a fair comparison to the proposed model.

Figure 3.8 shows example v_{in} waveforms for the two models being compared. The piecewise model used in [47] is shown by the dotted grey line, and the model with

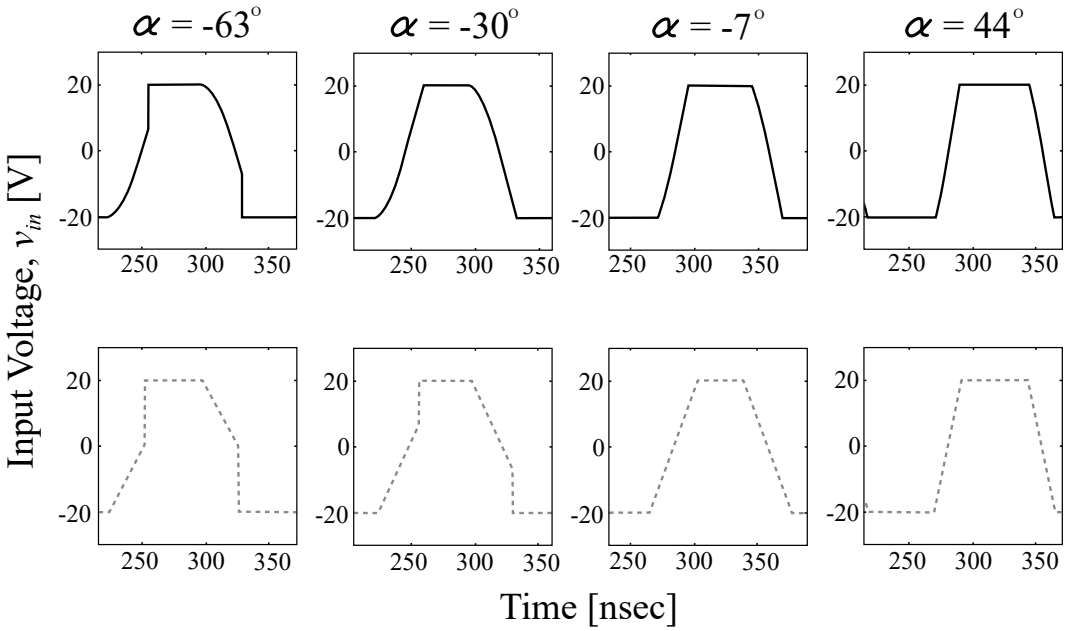


Figure 3.8: Comparison of waveforms using the precise (solid) and linear (dotted) modeling methods for V_{out}=20 V, i_{in}=0.75 A L_r=313 nH, and C_r=1120 pF.

the dead time i_L derived in (3.7) is shown in black. Given the different dead time transitions, the models will have different harmonic distributions, an important point for fair comparison. With an ideal LC resonance at the receiver coil, everything but the fundamental is attenuated. When considering only the fundamental component, this difference in harmonic distribution also means the rectifier's input phase will be different between the two models given the same value of α. This issue is relevant within both the comparison of waveform models discussed here and the experimental validation discussed later. For this reason the variable ϕ is introduced as the rectifier's fundamental input phase,

$$\phi = \angle v_{in\_fund} - \angle i_{in\_fund}, \tag{3.10}$$

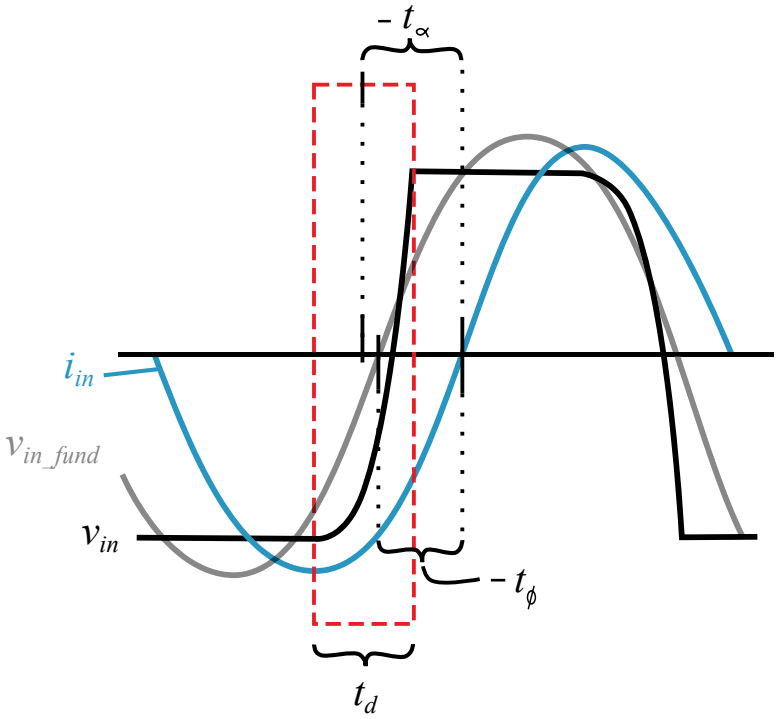
where v_{in_fund} and i_{in_fund} are the fundamental components of v_{in} and i_{in} respectively. The time representation of ϕ is given by

$$t_\phi = \phi/\omega_s. \tag{3.11}$$

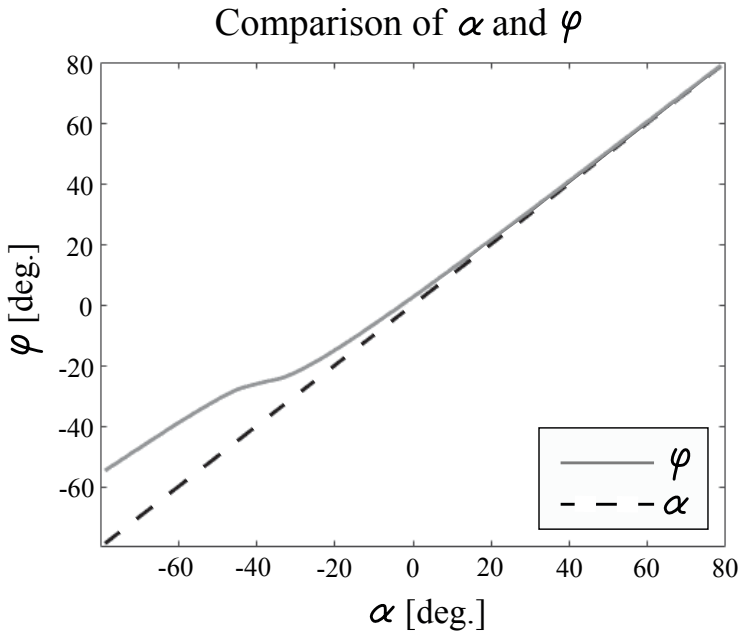
ϕ is used as a fair point of comparison for the precise and linear models. For clarity, ϕ is closely related to α, but the two ultimately do define different parameters. Figure 3.9a shows visually how α and ϕ are related. Figure 3.9b gives the precise relationship between the variables for the operating point used throughout the remainder of this section. The value of ϕ converges at largely positive values of α because the zero crossing of the fundamental component approaches the middle of the dead time.

In reference to Figure 3.8, notice that ZVS points first occur at different values of α (-30° and 7° for the improved model and the linear model, respectively). Also note that the models begin to look very similar for larger values of α. The area where the models begin to look the same is also the region where ϕ converges to α. Next, ϕ is used to contrast the linear and precisely derived dead time models.

Figures 3.10, 3.11, and 3.12 show the difference in the two models for THD, dead time, and input power respectively. Characteristics like conduction losses, efficiency, and output power also show differences when compared between these two models. Simply put, the proposed model is more accurate.



(a)



(b)

Figure 3.9: (a) Visualization of how α relates to ϕ and (b) graph of specific relation for V_{out}=20 V, i_{in}=0.75 A L_r=313 nH, and C_r=1120 pF using the precise dead time model.

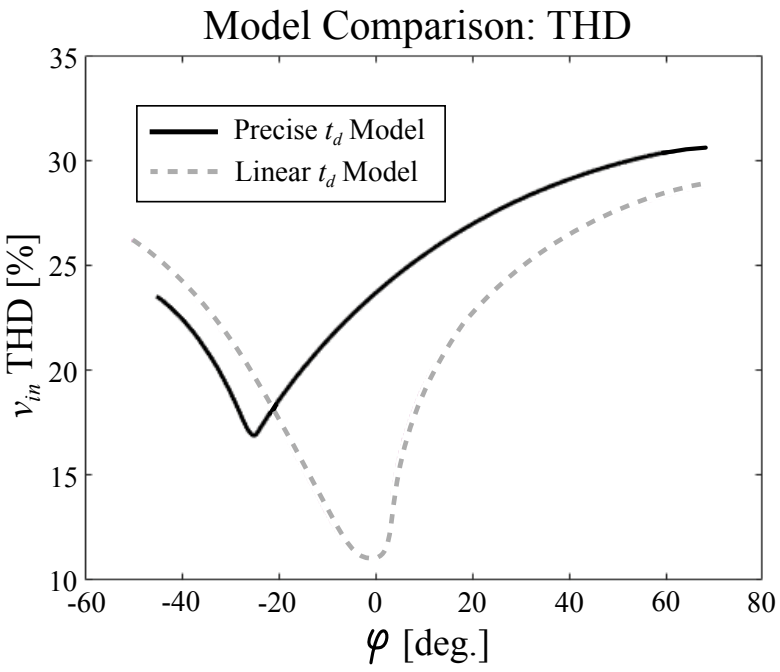


Figure 3.10: THD comparison of modeling methods for V_{out}=20 V, i_{in}=0.75 A L_r=313 nH, and C_r=1120 pF.

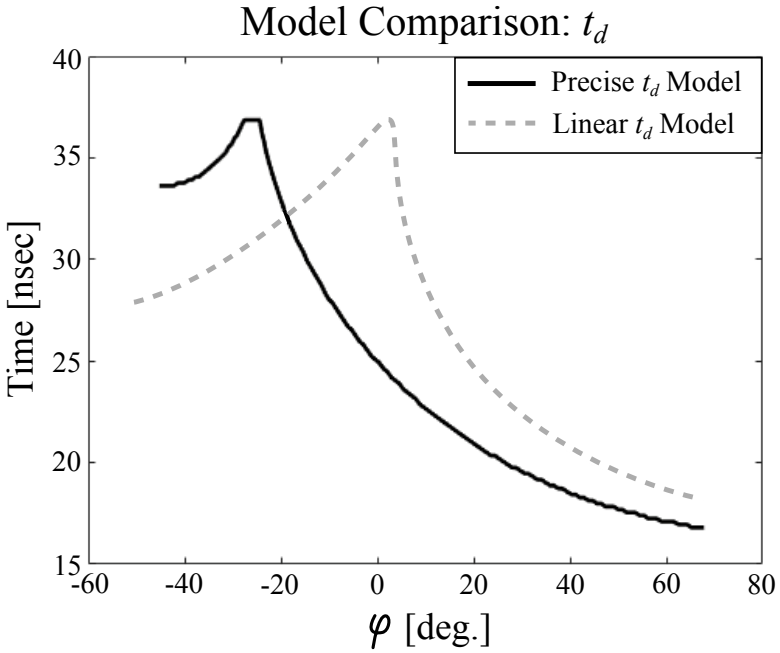


Figure 3.11: Dead time comparison of modeling methods for V_{out}=20 V, i_{in}=0.75 A L_r=313 nH, and C_r=1120 pF.

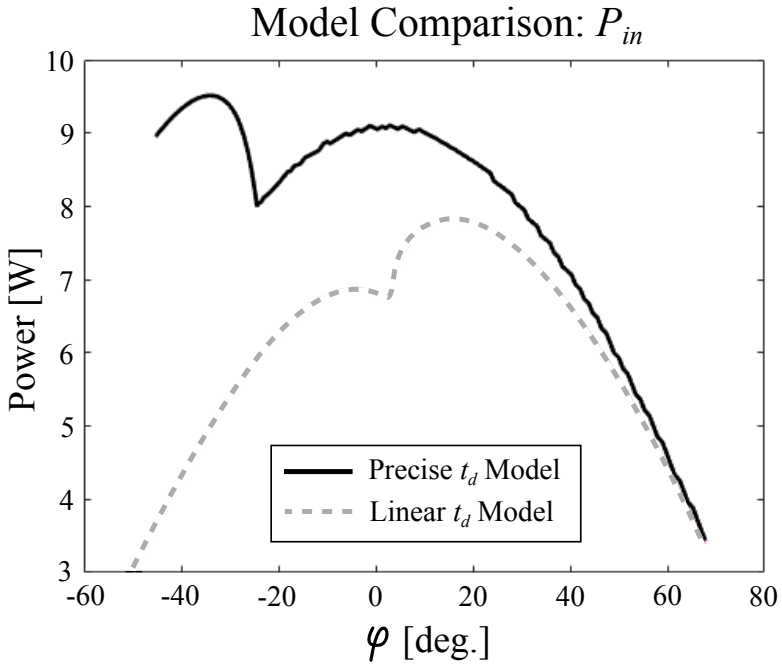


Figure 3.12: P_{in} comparison of modeling methods for V_{out}=20 V, i_{in}=0.75 A L_r=313 nH, and C_r=1120 pF.

If a designer was building the circuit for a given THD, both the inaccuracy at individual values of ϕ and the slightly different trend lines in Figure 3.10 could be an issue. Similarly, Figure 3.11 shows that the imprecise dead times of the linear model vary by as much as 10 nanoseconds in certain cases. Recall that the valleys of Figure 3.10 are the values of ϕ wherein ZVS is first achieved. The example in Figure 3.11 has the precise model predicting the ZVS point at a value of $\phi \approx 25°$. The linearized model predicts that ZVS will first occur at $\phi \approx 0°$. When an engineer is building a design that warrants a specific range of input phase control, this difference is critical. These examples show the necessity of both the precise modeling method and equation (3.7), upon which the model is built.

The linear model is built upon the assumption that the input current, i_{in}, is small compared to the resonant current, i_L, during the dead time. This is especially true for large values of $+\phi$. Note that at large values of $+\phi$ the models approach one another for THD, dead time, and input power. This shows that both models are functioning correctly. The degree of deviation between the two models implicitly shows the degree to which the assumption of the linear model holds for the power level and tank design of this particular simulation. Overall, these examples illustrate that deriving the precise dead time characteristics equips the proposed model for improved accuracy and precision. Next, it is important to use the improved model to help make circuit design decisions.

3.5 Choosing L_r and C_r

The proposed code model is used to sweep the L_r and C_r parameters. Variables L_r and C_r influence system efficiency, THD, output power, and dead time. In general, all of these characteristics are interdependent, making design without simulation significantly more difficult. However, the ability to map the L_r and C_r design space quantifies and, consequently, simplifies the design process.

Figure 3.13 shows how the THD changes for a single value of α, V_{out}, and I_{in} given different resonant tank designs. The red dotted line shows the space where THD tends to be the lowest, with the overall lowest THD occurring near large values of C_r and small values of L_r. The v_{in} waveforms of both the bottom left and the

top right corners of Figure 3.13 approach square waves. These corners resonate too quickly and too slowly, respectively.

Figure 3.14 shows the same data as Figure 3.13 in terms of characteristic impedance and resonant frequency. The red dotted line showing the valley of lowest THD values occurs near a single resonant frequency. The parameter that is largely changing along the red dotted line is the characteristic impedance of the resonant tank.

The L_r and C_r design space is described in terms of efficiency. In the bottom left corner of Figure 3.15 where L_r and C_r are small, the circulating current will be high, and I^2R losses will be large. Similarly, in the top right corner of Figure 3.15 where L_r and C_r are large, ZVS cannot be achieved and the hard switching losses become overpowering. These dynamics correspond to the THD graph of Figure 3.13, once again pushing design toward the red dotted line.

Figures 3.16 and 3.17 also give insight into choosing L_r and C_r. Figure 3.16 gives the total range in degrees from $\alpha = 90°$ to the point where ZVS is lost. This ZVS range is considered to be the usable input range of α because the switching loss without ZVS is large. While an engineer could choose to operate outside this range, the presence of C_r further increases the losses of hard switching actions, discouraging operation in this region even more so. Furthermore, the model does not support the parasitic elements necessary to simulate ringing, and consequently, the simulated THD calculations are not expected to match experimental results for hard switching waveforms. The point at which ZVS is achieved is the also the value of α at which a

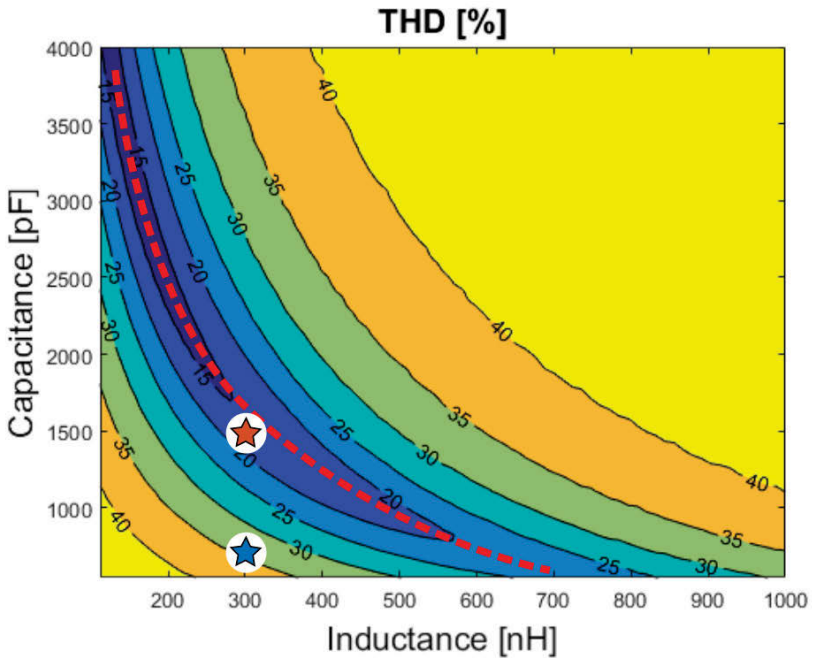


Figure 3.13: Graph of THD within the L_r and C_r design space for V_{out}=15 V, i_{in}=0.75 A, and α=0°. The optimal THD trajectory and the two test points of Figure 3.18 are shown.

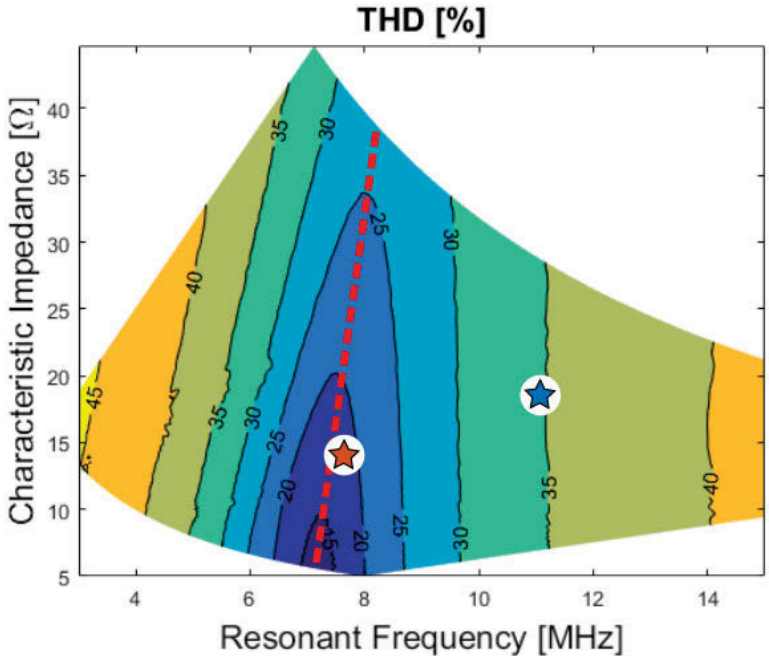


Figure 3.14: Graph of THD within the ω_0 and R_0 design space for V_{out}=15 V, i_{in}=0.75 A, and α=0°. The optimal THD trajectory and the two test points of Figure 3.18 are shown.

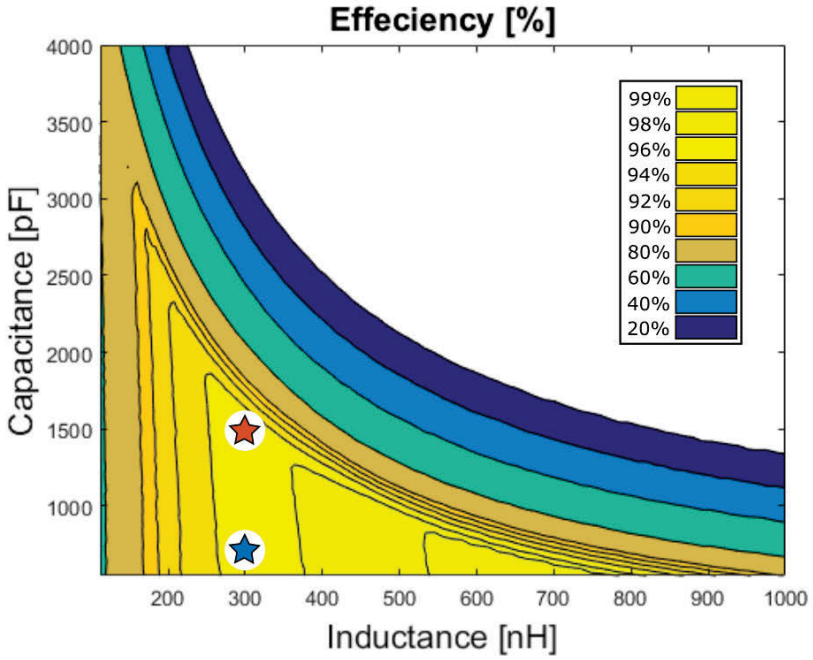


Figure 3.15: Graph of efficiency within the L_r and C_r design space for V_{out}=15 V, i_{in}=0.75 A, and α=0°. The test points of Figure 3.18 are shown.

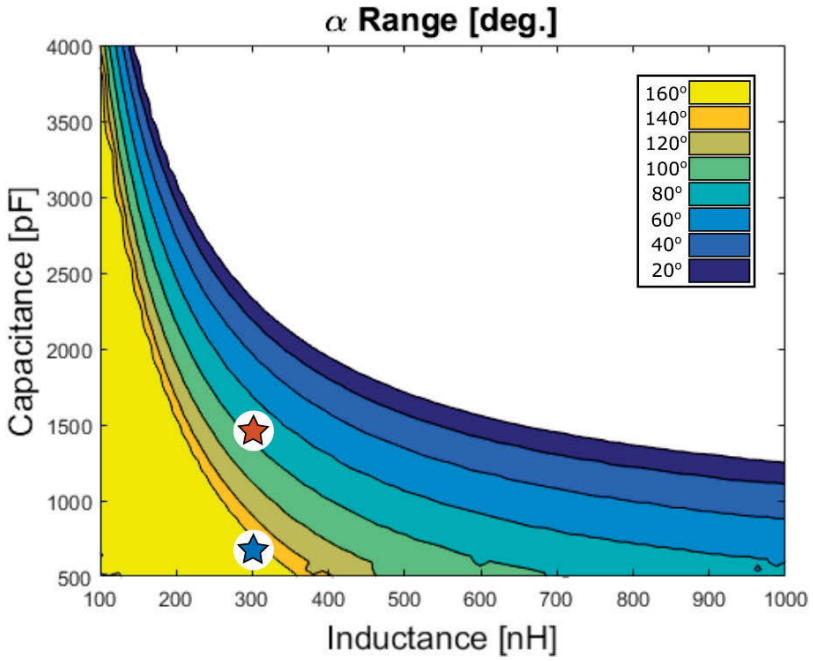


Figure 3.16: Graph of the α range within the L_r and C_r design space for V_{out}=15 V, and i_{in}=0.75 A. The test points of Figure 3.18 are shown.

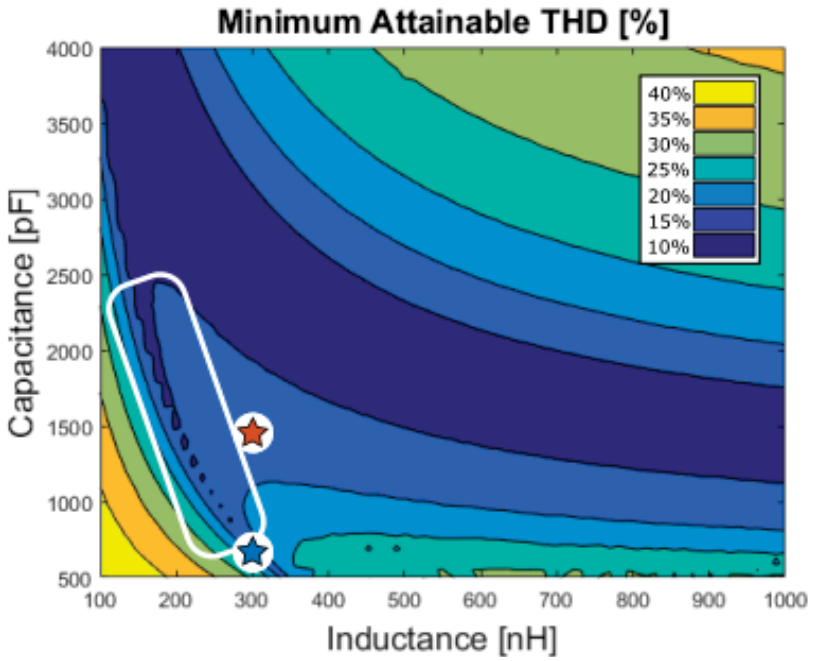


Figure 3.17: Graph of the minimum attainable ZVS within the L_r and C_r design space for V_{out}=15 V, and i_{in}=0.75 A. The test points of Figure 3.18 are shown.

design will observe its lowest THD value. A graph showing the minimum attainable THD values is shown in Figure 3.17. By combining the characteristics of THD at $\alpha = 0$, efficiency at $\alpha = 0$, minimum THD, and α range, the tradeoffs connected to a designer's choice of L_r and C_r begin to take form. Generally, a larger amount of phase control will warrant a larger THD, and the lowest THD designs will decrease efficiency and phase control.

Because of these characteristics, the tank should be chosen after the specific design application is established. A designer must first identify the requirements for the the system under construction, and using those parameters, the circuit can be designed with an understanding of the "cost" of each decision. For instance, a rectifier that needs above 97% efficiency and below 20% THD at a single input phase might choose

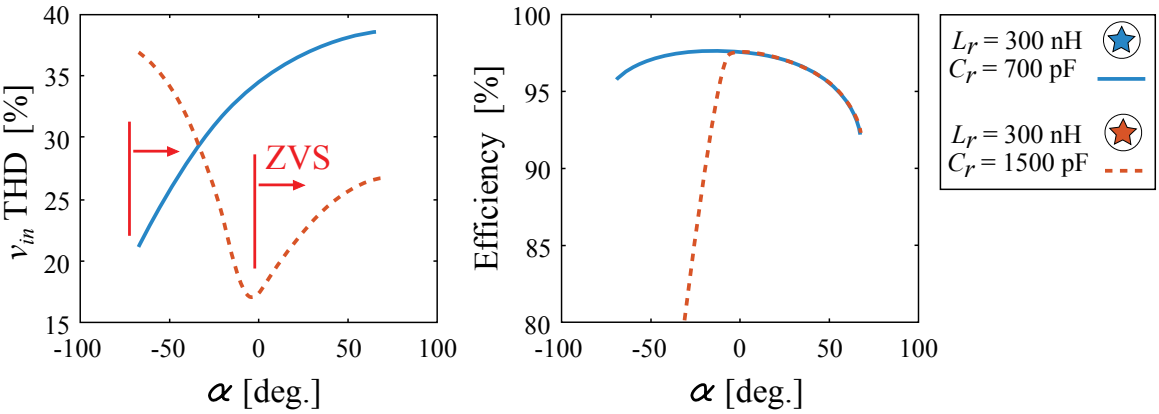


Figure 3.18: Comparison of the tank designs marked in Figures 3.13-3.17. V_{out}=15 V and i_{in}=0.75 A.

L_r=300 nH and C_r=1500 pF as shown in Figure 3.18. A different design that needs the same efficiency levels but much more phase control must sacrifice THD levels to do so. An example of this design using L_r=300 nH and C_r=700 pF is also included in Figure 3.18. These two design points are also marked by stars on Figures 3.13-3.17.

In Figure 3.17, the section of data outlined by the white box is generated by an unexpected mechanism. This data trend can be addressed by inspecting the THD graphs of individual data points. The "minimum attainable THD" is acquired by comparing the THD levels of each value of α used in simulation. The lowest value from this data set shows up in a manner similar to the "valley" in the THD graph in Figure 3.7a. The cause of the trend outlined in Figure 3.17 is that the lowest THD value is not assigned by a "valley." Rather, the edge of the simulation window holds the lowest THD. For these cases, the THD trend is still decreasing when the simulation iterates through its final value of α, rendering the "minimum attainable THD" different than the actual value. Overall, the oddity is easy to recognize and is a

function of finite sampling ability, not calculation error. Furthermore, the distortion occurs in a data range that is non-critical, and the general trends can still be extracted given a knowledge of what is causing the data misrepresentation.

The data presented in Figures 3.13-3.17 serves to illustrate how the proposed code-based modeling approach is able to provide quantitative insight into a designer's choice of L_r and C_r. The purpose of this approach is not to identify one optimal design as applied to any WPT system. Rather, the approach allows a designer to choose L_r and C_r to precisely fit his or her specific application requirements. In this way, intelligent choices can be made concerning the trade-off relationships of THD, efficiency, and phase control. The stars on Figures 3.13-3.17 and the corresponding graphs in Figure 3.18 are an example of how these resonant tank design tools might be utilized for two different design requirements. This example illustrates that more than one viable design exists, and the criteria for naming the optimal design is contingent upon the specific application requirements.

3.6 Summary

The basic waveforms and operation of the proposed rectifier are described, and a solution of the input-phase-dependant resonant dead time transition is provided. The precisely derived dead time transition is used to build a circuit model in MATLAB. This model is compared to a model with a linearized dead time in order to illustrate the significance of the precise dead time derivation. Finally, the proposed modeling

method is used to quantify the L_r and C_r design space in terms of THD, efficiency, and α, and an explanation of the tradeoffs among the design characteristics is given via two valid resonant tank designs.

Chapter 4

Experimental Verification

The design process for the experimental board included three iterations of PCB design, each improving on issues highlighted by the previous. Consequent of this process, two practical considerations are analyzed. These two are a discussion of the gate driver choice for the gallium nitride devices and an evaluation of the circuit's parasitic elements. Following this, the experimental setup is shown and explained, and test results are used to validate the modeling method proposed in Chapter 3. Finally, the difficulty in attaining precise measurements when the waveforms have characteristics similar to those of P_{in} is discussed.

4.1 Experimental Setup

In order to validate the model, an experiment is set up for testing the proposed circuit. The prototype results showcased in this section are from the third PCB

board. The rectifier operates at P_{out} = 20 W, V_{out} = 20 V, $I_{in} = 0.75A$ A, and it has L_r and C_r values of 313 nH and 1120 pF respectively. The input current of the experimental set up is supplied by a 75 W power amplifier, model number 75A250A. The power amplifier signal is filtered by a 6.78 MHz series L - C to ensure a nearly sinusoidal input current signal as assumed by the model. The filter substitutes for the tuning of the receiver coil in a real WPT system. The input voltage and input current waveforms are measured between the filter and the proposed circuit. The proposed circuit uses EPC2016C FET devices. Each GaN device is driven by an LM5114 gate driver, and the PWM signals are delivered to the gate drivers by an Altera EP4CE22F17C6N FPGA.

The tests are administered in open loop. Two function generators are used in the test setup. One function generator sends a 6.78 MHz sine wave to the power amplifier input, and the other sends a 6.78 MHz square wave reference signal to the FPGA. The two function generators share a clock signal so that there is no frequency mismatch between them. Using the interface on the function generators, the phase shift between the two signals is controllable. This capability establishes control of the variable α for any set of conditions under test.

The power amplifier has a gain control nob that allows for real-time tuning of input power levels. Extra fine tuning of these power levels can be done by changing the amplitude of the sinusoidal signal entering the power amplifier from the function generator. An electronic load is connected to the output DC bus of the rectifier. The

electronic load is capable of acting as a constant resistance, voltage, current, or power load. For many of the tests conducted in this work the load is fixed as a voltage sink.

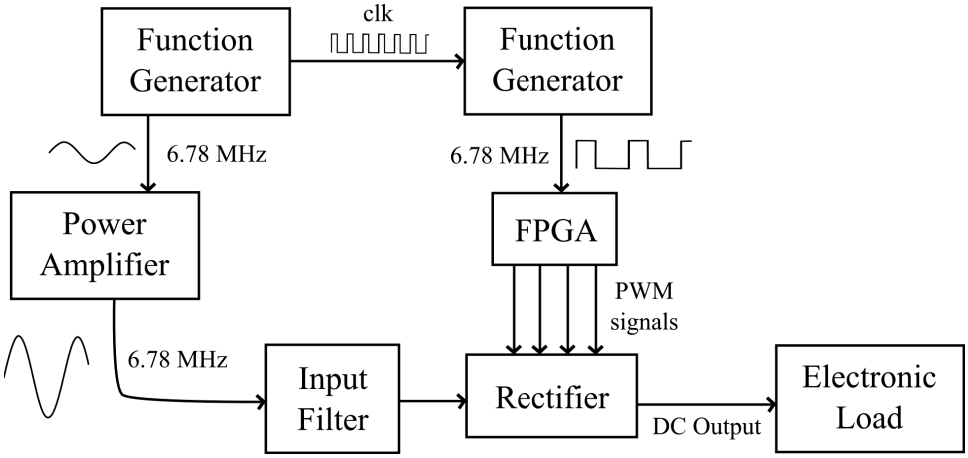


Figure 4.1: Open loop experimental testing scheme using two function generators.

Figure 4.1 illustrates how the components that comprise the experimental setup interact with one another. This system allows the test to achieve any reasonable V_{out}, i_{in}, and α. The circuit dead time, t_d, can be changed by editing the FPGA code. Figure 4.2 shows the components in the laboratory.

4.2 Gate Driver Choice

As mentioned in chapter 2, the half-bridge gate driver from Texas Instruments, the LM5113, is used in multiple high frequency GaN applications [41, 42, 44]. However, each of the listed applications is tested somewhere in the range of 800 kHz to 5 MHz, and consequently all are operating at a lower frequency than the WPT in this work. Furthermore, the combination of their power levels (100W, 60W, and 120W) and peak efficiencies (94%, less than 90%, and 89.2%) reveals that the losses

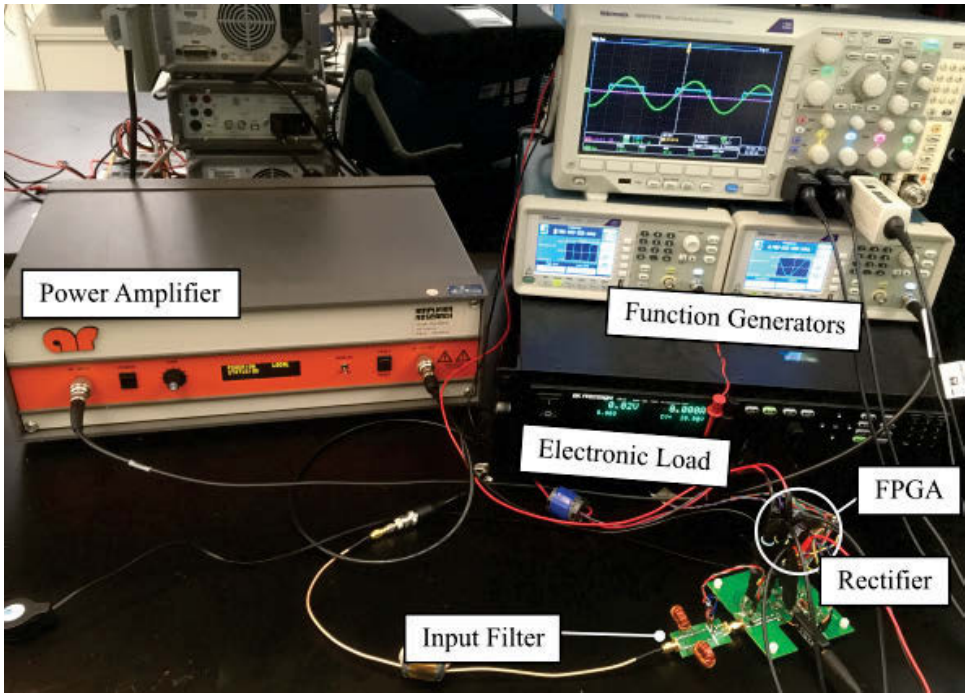


Figure 4.2: Experimental setup for open loop model verification.

of these studies are higher than the losses in this work [41, 42, 44]. This work operates at 6.78 MHz, generally has an output power of 20 W or less, and will often target efficiencies at or above 95%. For these reasons, the differences in switching frequency and observed loss, this work draws a different conclusion concerning the use of the LM5113 gate driver. The LM5113 is determined to be a sub-optimal solution for use in the WPT application of this thesis, as the driver's losses tend to dominate at low powers, higher voltages, and high switching frequencies.

Figures 4.3 and 4.4 show a thermal image of the first PCB iteration of the proposed circuit as implemented with the LM5113 gate driver. The circuit in Figure 4.3 is operating at 8.38 W, and the gate drivers are significantly hotter than the rest of the board. Furthermore, the temperature gradient implies that most of the heat in the

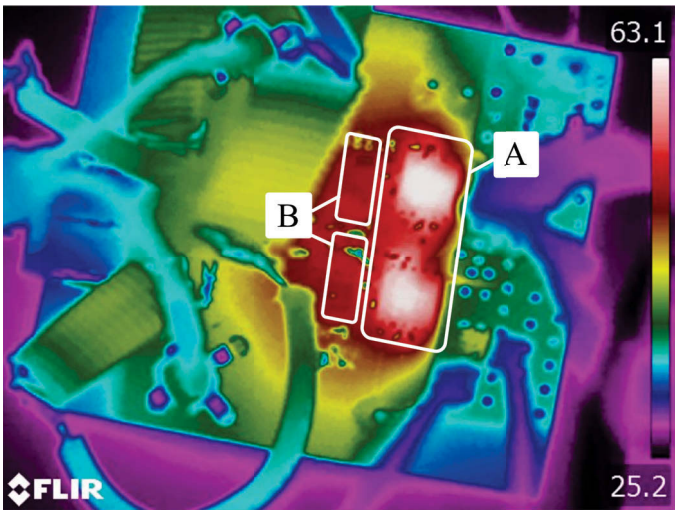


Figure 4.3: Early board iteration with high gate driver temperatures relative to GaN devices at 8.38 W output. The image shows the (a) LM5113 gate drivers and the (b) GaN devices.

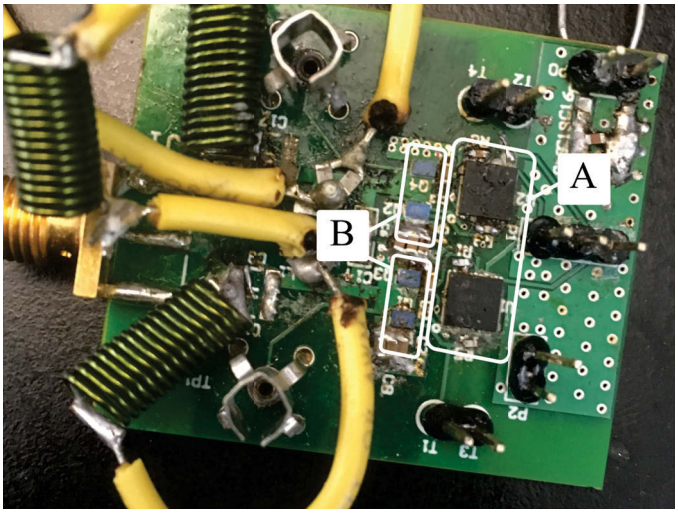


Figure 4.4: Picture of early board to match the thermal image showing (a) GaN devices and (b) LM5113 gate drivers.

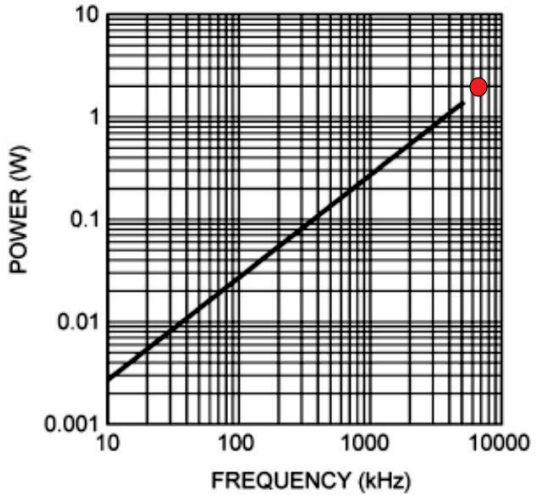


Figure 4.5: LM5113 reverse recovery loss for V_{IN}=50 V and Q_G=10 nC [3] [edited].

switching devices originates in the gate drivers. The loss implications of Figure 4.3 are confirmed by the LM5113 datasheet. Gate driver losses include CMOS dissipation, bootstrap forward conduction loss, and bootstrap reverse recovery loss. Among these, reverse recovery is shown to be dominant in the datasheet when 50 V and 6.78 MHz are the output voltage and switching frequency, respectively [3]. Figure 4.5 shows the expected LM5113 loss due to reverse recovery for an example case.

Notice that the graph only shows data up to 5 MHz, and at 5 MHz the losses are already greater than 1 W [3]. The red dot on Figure 4.5 is where 6.78 MHz would appear on the trend line, and at this dot, there are 2 W of loss due to reverse recovery. At the operating point shown in Figure 4.3, 4 W of gate driver loss (2 W per driver) is much larger than the total loss of the rest of the power circuit. Again, this is not the case for the works cited [41, 42, 44]. To avoid these losses, second and third generation boards are constructed with LM5114 gate drivers, one per switching

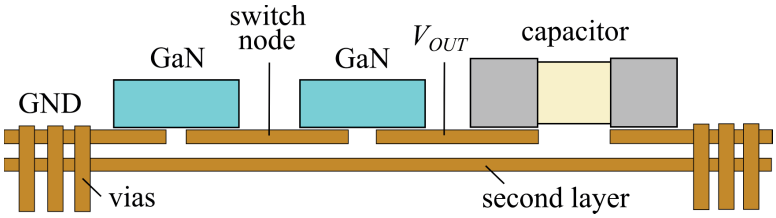


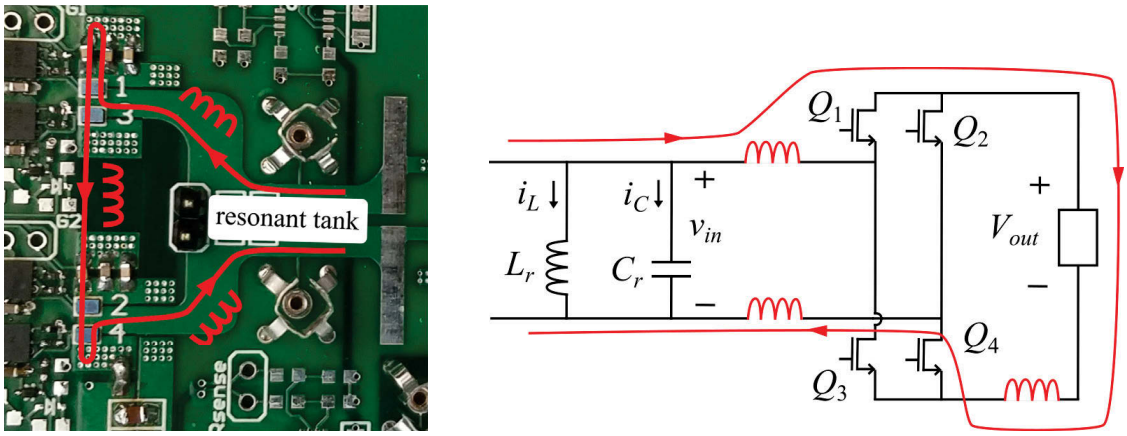
Figure 4.6: Second PCB half bridge layout minimizing loop inductance.

device. This allows design of the bootstrap circuitry external to the gate driver. A 200 mA, 0.3 V schottky diode is used for the boostrap diode in order to avoid reverse recovery mechanisms. Overall, the gate drivers are much cooler at low power, implying that reverse recovery was the dominant cause of gate driver loss.

4.3 Parasitic Inductance

At 6.78 MHz, parasitic elements previously considered negligible can no longer be ignored. Parasitic inductance is especially detrimental in high-current traces. On the second PCB, the power loop layout of each half bridge is carefully laid out with decoupling caps, minimizing the inductance at high frequency as illustrated in Figure 4.6.

Although the loop shown in Figure 4.6 has sufficient parasitic reduction for the very high frequency content of switching actions, other board parasitics on the second PCB are significantly detrimental. At 6.78 MHz the fundamental rectifier input signals are susceptible to substantial parasitic-induced distortion. Both the distance between each half bridge and the distance from the full bridge to the resonant tank are too large. Each of these relatively large distances creates a parasitic inductance



(a) (b)

Figure 4.7: (a) Second PCB layout, example power current path, and corresponding parasitic inductances, and (b) circuit diagram with same current path and parasitic inductances.

that significantly distorts the rectifier input voltage and raises the THD, undermining a major benefit of the proposed circuit.

Figure 4.7a shows the second PCB board zoomed to the GaN switches and resonant tank. An example current path flows from the input of one switch node through Q_1, down through the vias and second layer trace to Q_4, and back to the resonant tank through the second switch node. The parasitic inductances are shown on Figure 4.7a and correspond with long stretches of copper trace on the PCB layout. The same current path and parasitic inductances are shown in the circuit diagram of Figure 4.7b.

The parasitics shown in Figure 4.7 affect the input voltage of the rectifier. During the time when the switches are conducting, these parasitics create ringing around $\pm V_{out}$ at the input. Figure 4.8 shows an example case of rectifier input current and voltage at a 20 W operating point. Note how the resonant transitions appear to be

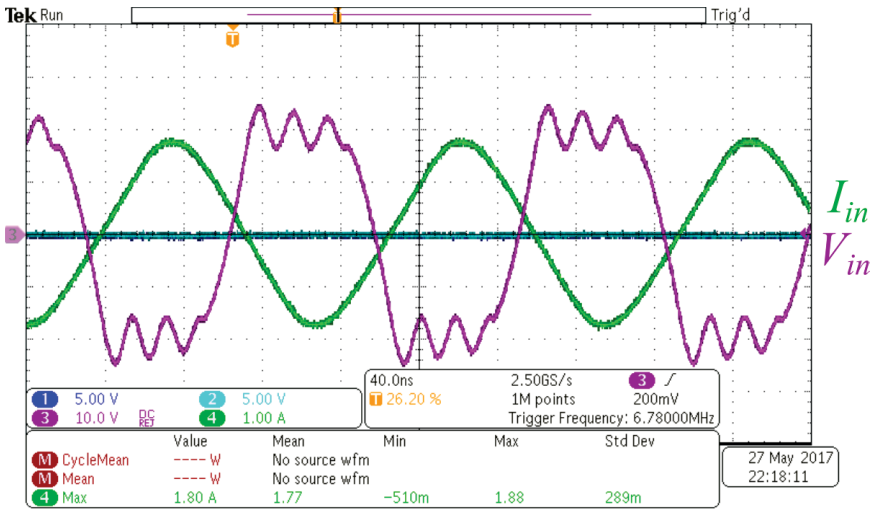


Figure 4.8: Second PCB input waveforms with large parasitic ringing at V_{out}=20 V and P_{out}=20 W. (The polarity of the v_{in} waveform was mistakenly flipped when the image was acquired. The true phase matches that of Figure 4.11.)

smooth, but during the power delivery intervals there exists a single frequency ringing centered around the DC operating point $\pm V_{out}$.

This ringing is addressed on the third PCB by minimizing the outlined parasitic inductances. The same half bridge high frequency inductance loop scheme is used, but the decoupling capacitors are moved to the middle as seen in Figure 4.9. The benefit of rearranging in this manner is that the switch nodes are now exposed on the ends of the layout, and the DC nodes are contained in the middle. This allows the resonant tank to be in very close proximity to the full bridge and for the half bridges to be in very close proximity to one another.

The layout of the third PCB is seen in Figure 4.10. The current loop during power delivery is substantially smaller than in the previous iteration of the board. With the reduction in parasitics, waveforms for the third PCB can be seen Figure 4.11. The ringing is smaller in amplitude and higher in frequency, both indicating a reduction in

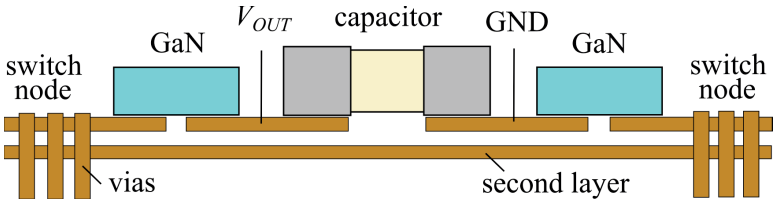


Figure 4.9: Third PCB slightly adjusted half-bridge layout with the purpose of moving the switch node to the edge of the loop.

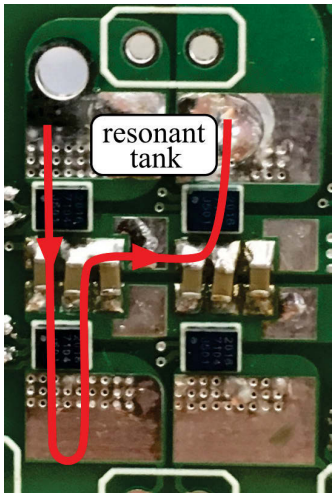


Figure 4.10: Third PCB with parasitic-reducing layout and example current path.

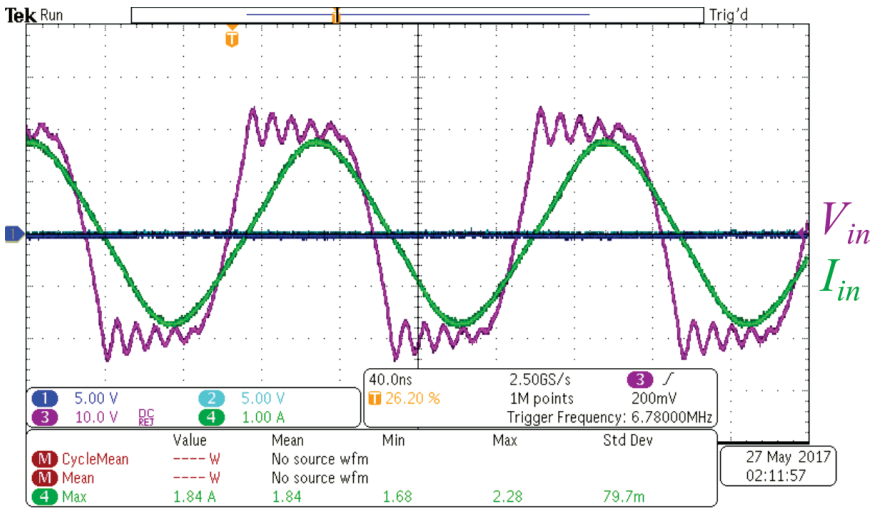


Figure 4.11: Third PCB input waveforms with reduced ringing, V_{out}=20 V and P_{out}=20 W.

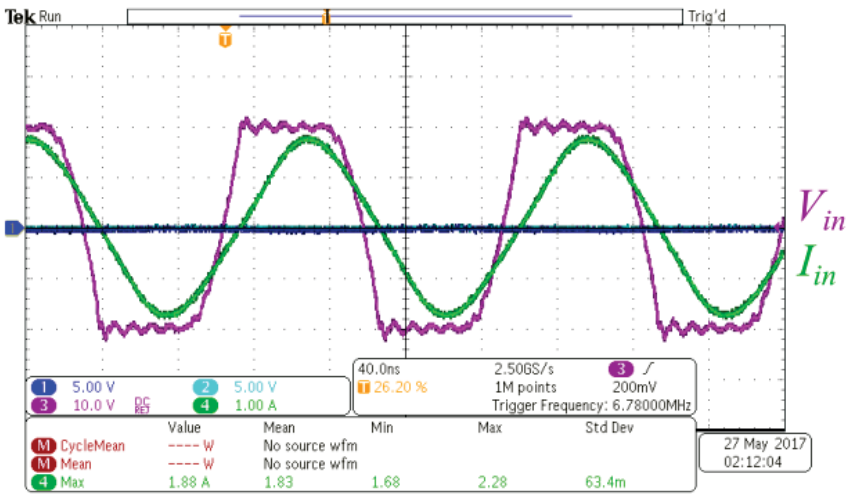


Figure 4.12: Third PCB input waveforms with reduced ringing as measured from optimal PCB location, V_{out}=20 V and P_{out}=20 W.

parasitic inductance. Both of these characteristics are beneficial in terms of harmonic distortion: the lower amplitude reduces the impact on THD, and the higher frequency means that this parasitic resonance is both better attenuated by the same filtering and less likely to increase harmonics near the fundamental. Practically, improving the parasitics on the board means that the experimental THD measurements will more closely match the modeled THD characteristics.

Depending on where one measures the differential input voltage, the parasitic effects are different. For example, measuring v_{in} near the resonant tank on Figure 4.7b is different than measuring near the switches (even though the two are ideally considered the same node). The same principle holds true for the third PCB, and although Figure 4.11 is shown as a fair comparison to the second PCB, Figure 4.12 is included to illustrate the same data point measured from a different PCB location. The waveforms in Figure 4.12 are measured with the differential probe placed on

the two lowest exposed switch node planes in Figure 4.10, while the waveforms from Figure 4.11 are measured with the differential probe placed around the "resonant tank" label of Figure 4.10.

4.4 Experimental vs. Modeled

Example waveforms are shown in Figure 4.13. As modeled, the input current is a sinusoid and the input voltage is $\pm V_{out}$ with resonant dead time transitions. The method for acquiring experimental data is as follows. The dead time is set in the FPGA code, and the electronic load is prepared to regulate at a fixed output voltage. Next, the input phase and input current level are adjusted using function generators and amplifier gain nob until the measured point matches the simulated point. The waveforms (like those in Figure 4.13) are saved from the oscilloscope (part number: MCO3104) and inserted into a MATLAB code. For each data point, the code calculates THD, input power, and ϕ.

Using the same circuit values for comparing the linear and precise models in Chapter 3, the experiment is conducted at an operating point with $V_{out} = 20$ V, $I_{in} = 0.75$ A, $L_r = 312$ nH, and $C_r = 1120$ pF. Figures 4.14a and 4.14b show that the THD and P_{in} data points follow the trends established by the proposed model. The experimental THD data seems to be higher than the proposed model by 2 to 4 percentage points, depending on the data point. This could be from the non-ideal ringing in the waveforms during the power delivery stage or noise that exists in real

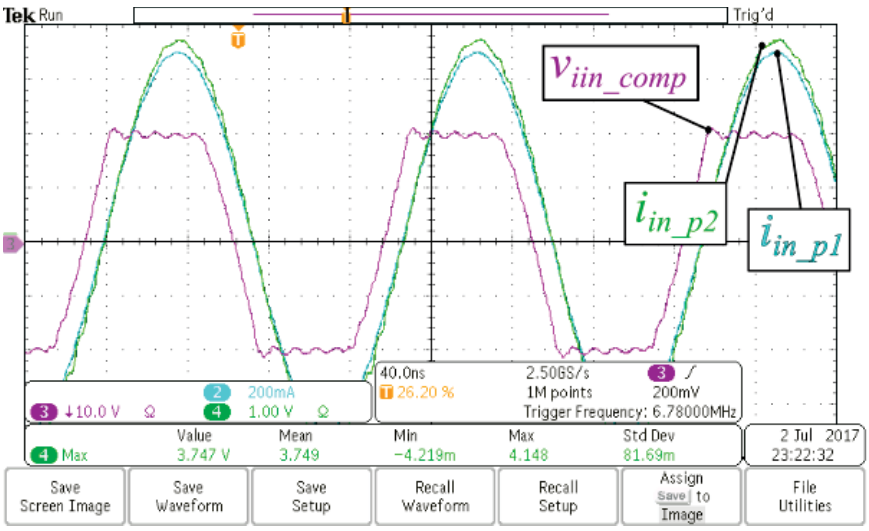
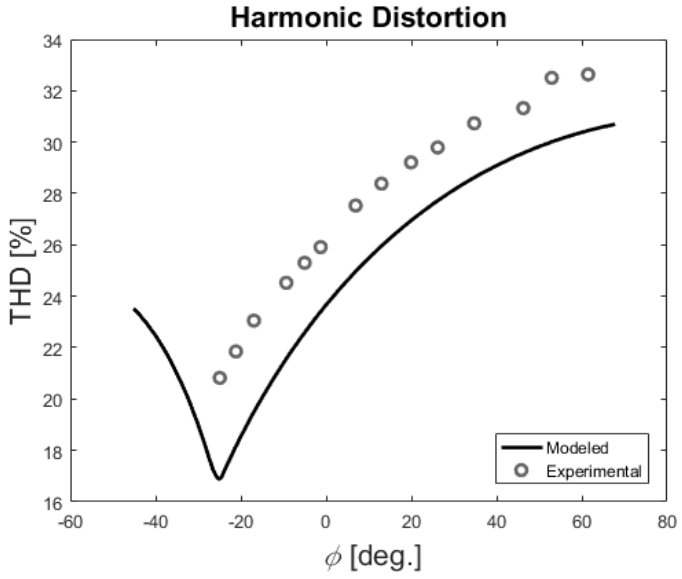


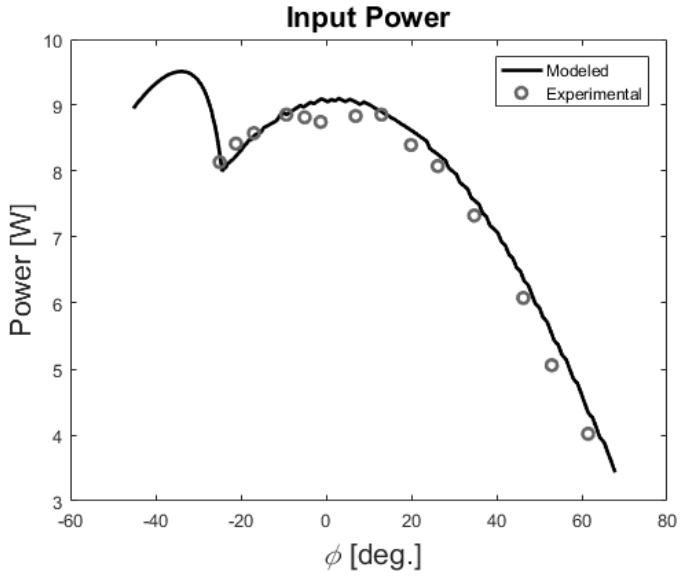
Figure 4.13: Example experimental waveforms showing measured v_{in} and i_{in}. $V_{out} = 20$ V, $I_{in} = 0.75$ A, $L_r = 313$ nH, $C_r = 1120$ pF, and $\phi = -24.95°$. Measurements from current probes numbered 1 and 2 in Figure 4.16 are shown, channels 2 and 4, respectively.

systems but is absent in the model. Nevertheless, the model derived in chapter 3 does a good job of predicting the trends of the proposed circuit.

One point of discrepancy in the experimental data is that of output power, P_{out}. This is especially curious because of the well-matched P_{in} trend displayed by Figure 4.14b. If P_{in} is predicted correctly but P_{out} diverges, then one would initially assume a modeling error. However, this fails to explain the observed trends. The experimental data for P_{out} is relatively well-matched at larger output powers, but the data points at smaller output power levels are lower than expected, as shown in Figure 4.15. This trend is worthy of inspection because, at low power levels, measurement precision becomes vital for accurate results, and a minor error in measured loss can severely alter efficiency calculations. For this reason, the probes used to obtain experimental results are examined.



(a)



(b)

Figure 4.14: Experimental data vs. modeled data for both (a) THD and (b)P_{in} where $V_{out} = 20$ V, $i_{in} = 0.75$ A $L_r = 313$ nH, and $C_r = 1120$ pF.

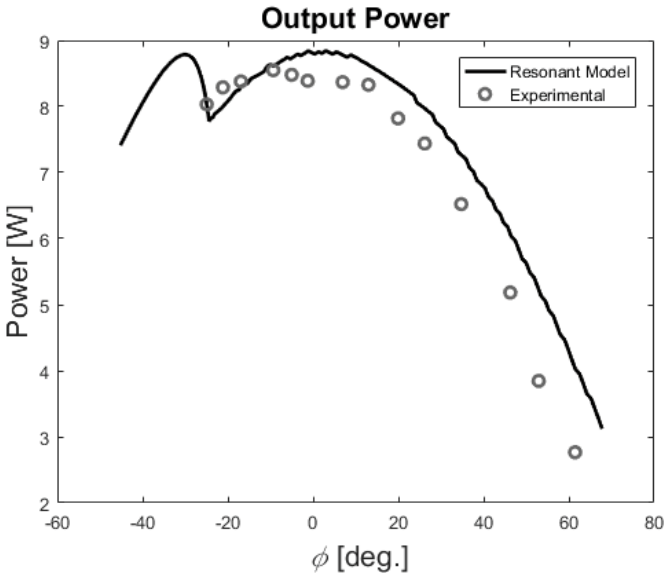


Figure 4.15: Experimental data vs. modeled data for P_{out} where $V_{out} = 20$ V, $i_{in} = 0.75$ A $L_r = 313$ nH, and $C_r = 1120$ pF.

4.5 Measuring 6.78 MHz AC Power

Accurate and precise power measurement of a relatively high frequency AC signal into an unmatched, dynamic load is difficult. Things like non-ideal dead times, imperfect input current peak levels and harmonic content, and probe non-idealities introduce measurement error when verifying analytical models. As outlined in the experimental process, the oscilloscope is used to measure input power.

The same test case is individually evaluated with two different current probes. Current probe 1 is part number TCP0030A and is rated for 120 MHz. The sampling rate of the oscilloscope for testing with probe 1 is 5.0 gigasamples/second. Current probe 2 is the CT-1 current transformer, and it is rated for 1 GHz. The sampling rate of the oscilloscope for testing with probe 2 is 2.5 gigasamples/second. With a lower sampling rate, the test with probe 2 is conducted with over 350 samples per period,

suggesting that sampling rate is high enough that it does not adversely impact the results.

Refer back to Figure 4.13. It shows a single test point being simultaneously measured by both probes. Probe 1 (waveform i_{in_p1} in Figure 4.13)is deskewed to the value recommended by the oscilloscope, and probe 2 (waveform i_{in_p2} in Figure 4.13) is deskewed such that the reported signal is in phase with probe 1. Probe 1 is a digital probe that displays current, and probe 2 is a current transformer that shows 5 mV for every 1 mA. The oscilloscope grid size is adjusted such that the two probes should show the same current waveform in Figure 4.13, but there is a measurement difference. This difference results in significantly different measured P_{out} values between the two probes.

Almost all efficiencies measured with probe 1 are >100%, an impossible result. Shown in Figure 4.16, probe 2 gives more realistic efficiencies (all <100%). Both probes are rated for frequencies at least two orders of magnitude above the fundamental frequency, but the results show significant deviation with regard to the precision necessary for a high efficiency, low power system.

This example of measurement error is one of many difficulties in experimental validation for low power and high frequency systems. For this reason, it is worthwhile to observe the circuit from a heat dissipation perspective in order to see if what is conveyed by the thermal images agrees with the measured points.

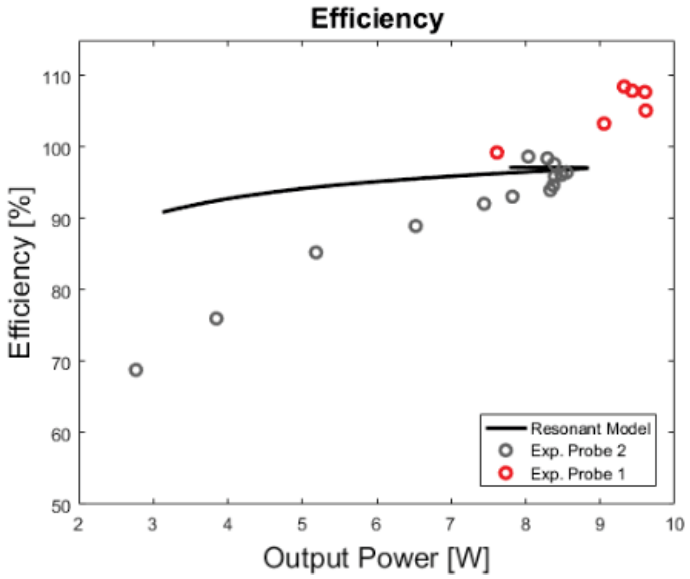


Figure 4.16: Experimental efficiency data overlaid on model simulations. V_{out} = 20 V, $i_{in} = 0.75$ A, $L_r = 313$ nH, $C_r = 1120$ pF

4.6 Thermal Characterization of Loss

Switches $Q_{1\text{-}4}$ and the resonant elements L_r and C_r are all shown in Figure 4.17. First, thermal measurements are taken while the circuit is performing rectification. Each thermal measurement is done with the camera (part number: T630sc) "spot" fixed on Q_2 for consistency. First, $Q_{1\text{-}4}$ are switched at 6.78 MHz, but the circuit is disconnected from input power. This test establishes a baseline temperature of around 39.4^oC. The roughly 14^oC rise from room temperature is due to both gate switching losses and heat that originates in the gate drivers and travels through the board to the switches. Neither of these losses is included in the model. The gate charge of a GaN device is considered to be small according to

$$P_{gate} = V_{gs} Q_g f = (5\ V)(3.4\ nC)(6.78\ MHz) = 0.115\ W, \tag{4.1}$$

Figure 4.17: PCB set up showing $Q_{1\text{-}4}$, L_r, and C_r.

and the gate driver operation losses are not included into the model because they are not part of the power stage losses. Next, two tests are evaluated at 10 W and 22.5 W. The 10 W test shows a Q_2 temperature of 57.8^oC, and the 22.5 W test shows a Q_2 temperature of 60.3^oC as can be seen in Figure 4.18. The changes in temperature, ΔT, are 18.4^oC and 20.9^oC respectively. The change in temperature is relatively small for a 125% power increase.

Next, the control test is done by shorting $Q_{1\text{-}4}$, and applying a DC current from V_{out} to the ground node. The temperature is monitored, and kelvin measurements are taken, giving insight into the relationship between power loss and temperature change. First, the test is run at zero current, marking the baseline temperature at Q_2 as 25.2^oC. Next, the power is adjusted until Q_2 has a temperature of 45.9^oC, making $\Delta T = 20.7^oC$. For this value of ΔT, the power losses are 470 mW, as can be seen in Figure 4.19. If the changes in temperature for the 10 W and 22.5 W tests are used to calculate their operating losses according to the trend established by this

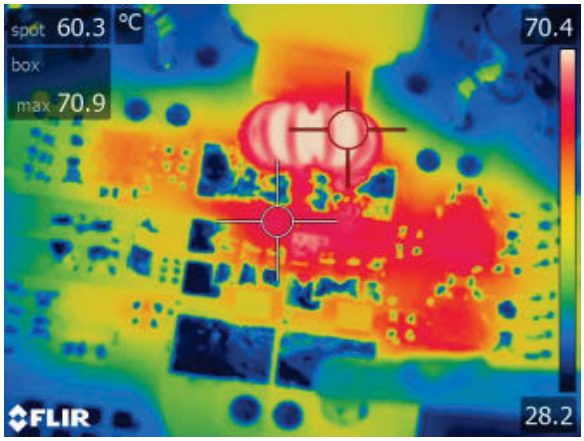


Figure 4.18: Thermal image of a test with $P_{out} = 22.5$ W, $V_{out} = 20$ V, $L_r = 313$ nH, and $C_r = 1120$ pF.

characterization test, then the efficiencies of the 10 W and 22.5 W tests are both >95%.

For comparison to the data in question, points are observed from Figure 4.15 at $\phi \approx 0^o$ and $\phi \approx 55^o$ using the same methodology. Based on both the experimental losses reported in Figure 4.15 and the control measurements taken, a simple thermal model would expect $\Delta T \approx 36^oC$. However, the ΔT is only $\sim 8^oC$, suggesting that the change in loss between the $\phi \approx 0^o$ and $\phi \approx 55^o$ operating points is much less than the experimental data reports. Assuming the high power tests are relatively accurate, the experimental deviation from the modeled output power in Figure 4.15 is less drastic than illustrated at low power. This result from thermal images, although imprecise, more closely agrees with what is modeled in Figure 4.15 than does the experimental data collected via the oscilloscope.

The implication herein is that the system operates more efficiently than the low-power data points of Figure 4.15 and 4.16 convey. This result also agrees with

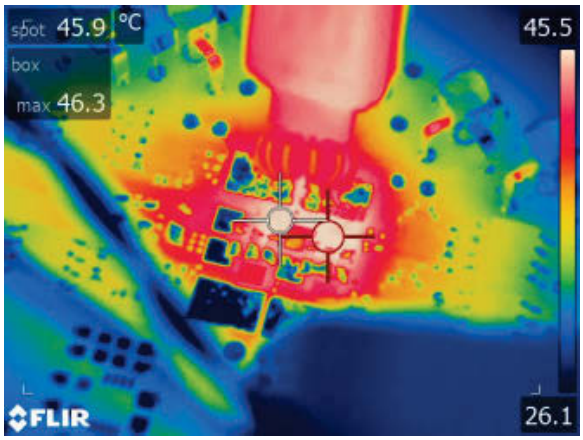


Figure 4.19: Thermal image of the test used to characterize the relationship between circuit loss and board temperature. There is 470 mW of loss at this operating point.

the assertion that high frequency, low loss, non-sinusoidal waveforms are difficult to measure with a high level of precision and accuracy. Awareness of this challenge is key for the correct design or characterization of any such system.

4.7 Summary

The experimental open loop setup is described, and the design choices concerning both the gate driver and the PCB parasitics are discussed. Experimental data is compared with modeled data, showing good agreement for P_{in} and the THD of v_{in}. The experimental data for P_{out} deviates from the model and warrants inspection. Two sufficiently rated current probes are tested, and it is found that each gives different values when measuring the same circuit waveform. The experimental data is then evaluated using thermal measurements, and the thermal measurements are a better fit to the model than the waveform measured results.

Chapter 5

Closed Loop Operation

This chapter discusses basic closed loop operation for the proposed rectifier. Fundamental closed loop operation is accomplished by feeding a sensed current signal to the FPGA that controls the gate PWM signals. Mechanisms used in establishing closed loop operation are discussed, and steady state operation is demonstrated.

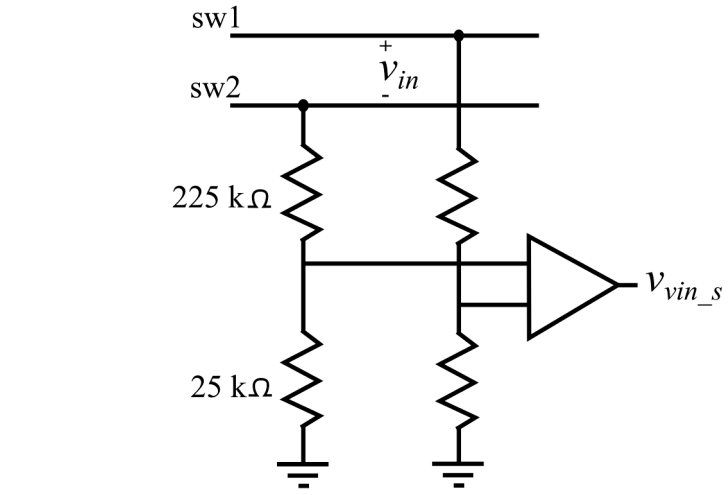
The closed loop implementation discussed in this chapter does not consider parameters like load step response, converter transfer functions, or loop gain. Each of these elements is related to output regulation. This chapter seeks to accomplish input phase regulation while addressing the problem of precisely synchronizing the switching rectifier to the input frequency. This is a non-trivial task, as even a 1 mHz difference between fundamental frequency and switching frequency causes gradual accumulation until the system is at an undesirable operating point.

5.1 Sensing Circuitry

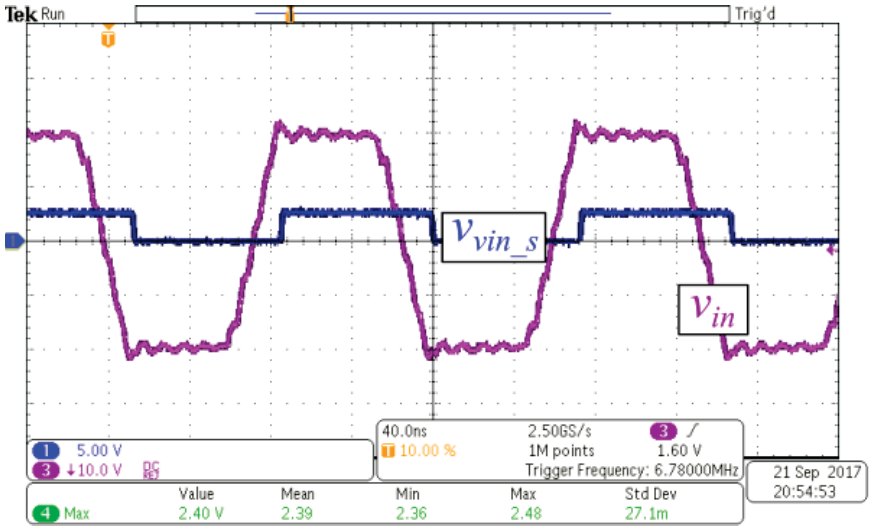
Steps are taken to establish closed loop control of the synchronous rectifier. The ability to regulate the input to the desired phase is achieved via closed loop operation. One large challenge associated with closing the loop is sensing the circuitry. Current sensing and high frequency sensing are both difficult, and combining the two into a single circuit sensing problem creates a significant challenge. Furthermore, because the circuit needs to regulate phase, the zero crossing detection must be accurate enough for a control circuit to regulate input voltage phase relative to input current phase.

The voltage and current sensors generate square waves with rising and falling edges that correspond to the rectifier's differential input voltage and current zero crossings. At a control level, the input voltage waveform is phase shifted via the controllable timing of switching signals. The current sense comparator is fed to an FPGA, and the FPGA times the switching signals such that input voltage is regulated to the proper phase.

The comparator used in this study is the LTC6752-2, a 280 MHz rated comparator designed with 1.2 ns rise/fall times and 2.9 ns propagation delays. Another important feature of the comparator is that this propagation delay does not heavily deviate with temperature or input common mode. These properties allow the sensing square wave to more closely align with zero crossing events, approaching the ideal case. The LTC6752-2 makes voltage sensing relatively straightforward. The rectifier's two



(a)



(b)

Figure 5.1: Voltage sensing (a) circuit and (b) waveforms.

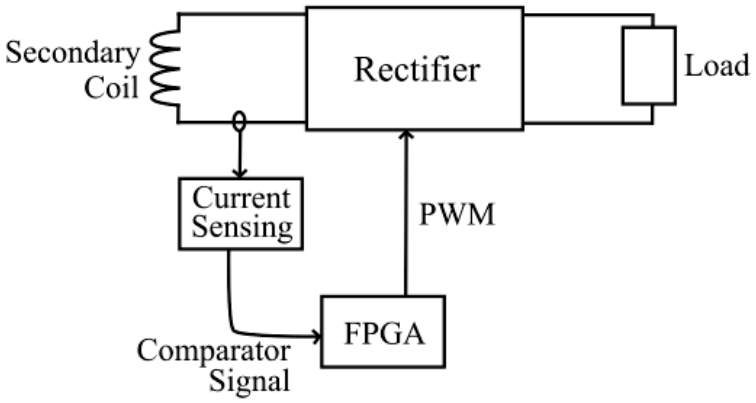


Figure 5.2: Basic closed loop configuration.

switch nodes are connected to a pair of resistor dividers as seen in Figure 5.1a. The dividers step the voltage down such that the input to the comparator is large enough to be well above circuit noise but small enough that the comparator is not outside its rated condition. The voltage divider is designed for a maximum input of 50 V, and because the peak of v_{in} is ideally equivalent to V_{out}, this means that the voltage sensing is designed with V_{out} considered. Figure 5.1b shows the rectifier's differential input voltage, v_{in} and the output of the sensing comparator, v_{vin_s}. The few nanoseconds of offset between the signals can be accounted for in the FPGA code.

Sensing the input current is much more difficult to achieve. The goal is to sense input current such that the sensing signal can be used for control as shown in Figure 5.2. Originally, current sensing was attempted by placing a sensing resistor at the output of the circuit before the large DC filtering capacitors. The idea was to sense the rectified sinusoidal current. This implementation was designed into the layout of the second PCB, but the technique failed when the high frequency decoupling capacitors largely smoothed the signal prior to the sensing resistor. Thereafter,

sensing attempts were made by placing the sensing resistor at the input of the circuit, but this failed due to noise distortion and power dissipation levels in the sensing resistor that were too high.

The solution can be seen in Figure 5.3. A current sensing transformer is added at the input of the rectifier. The effective load at the secondary is large, so the rectifier circuit sees only the magnetizing inductance of the transformer. The magnetizing inductance of the transformer is about 45 nH. The voltage across that magnetizing inductance is reflected across the isolation barrier to the 2.55 kΩ resistor before it is filtered by a balanced RC network. The network must be balanced to ensure a symmetrical output signal and to avoid activating the comparator's internal diodes located at each of the input pins. The RC network filters high frequency noise and steps down voltage. At the fundamental frequency of 6.78 MHz, the 10 pF capacitor is 2.35 kΩ of impedance, creating an impedance division between the 2.3 kΩ resistor and the 10 pF capacitor. The 20 kΩ resistor is added to keep from having infinite low frequency gain.

One significant issue with this sensing method is the 90° inductive phase shift of the sensing transformer. This problem is also accounted for within the design of the filtering network. The filter serves to phase shift the signal in a capacitive manner. Other parasitic capacitors and the delay of the comparator serve to further shift the signal. The total phase shift of the signal after this filtering process is close to 180°. This 180° phase shift is acceptable because the zero-crossings of i_{in} still align with the zero-crossings of v_{iin_s}. The end result of this process can be seen in Figure 5.4.

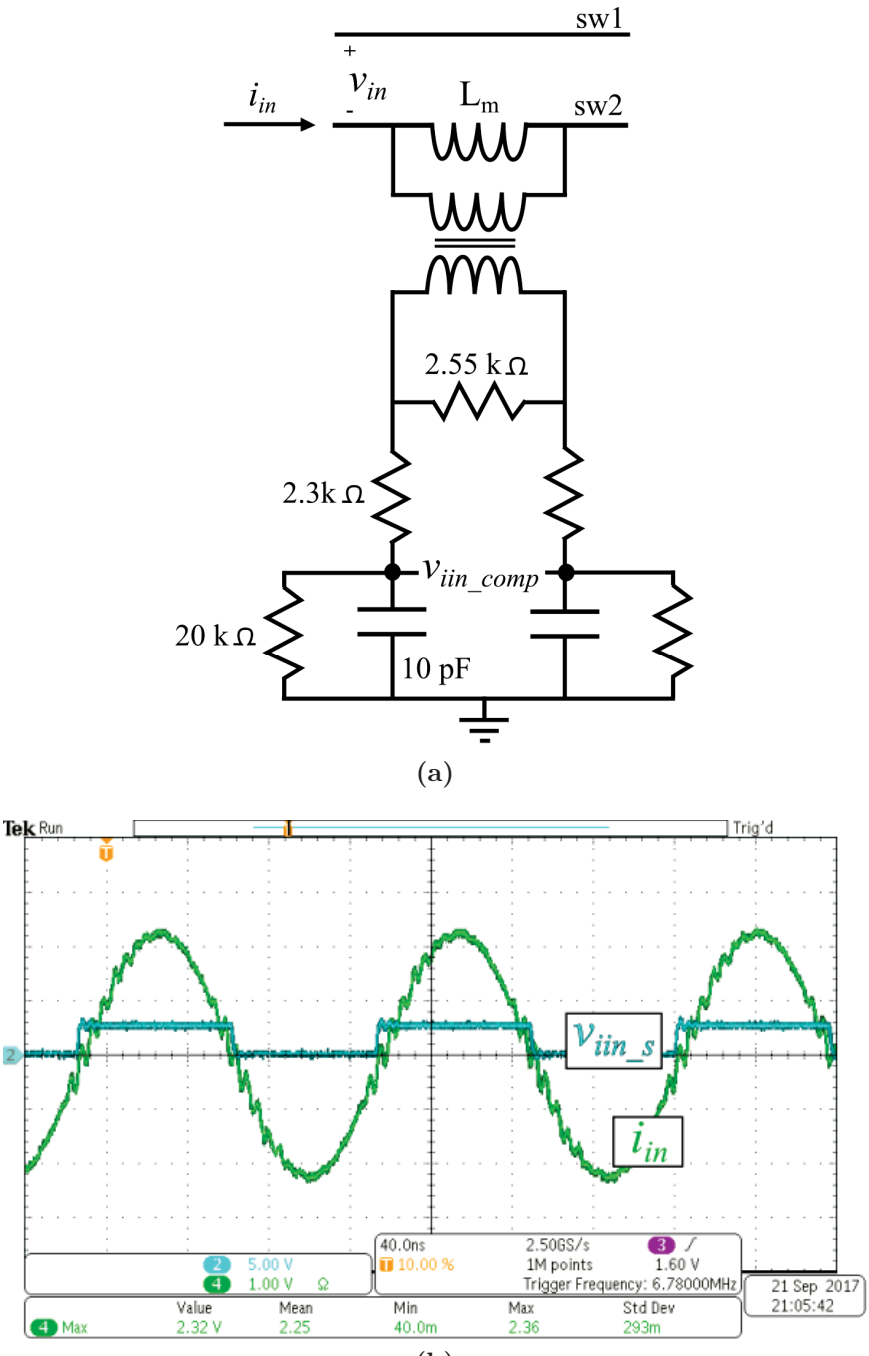


Figure 5.3: Current sensing (a) circuit and (b) waveforms. Waveform i_{in} is measured with a 50 Ω terminated current-sense transformer and consequently has scale units of voltage. The conversion ratio is 1 V to every 0.2 A.

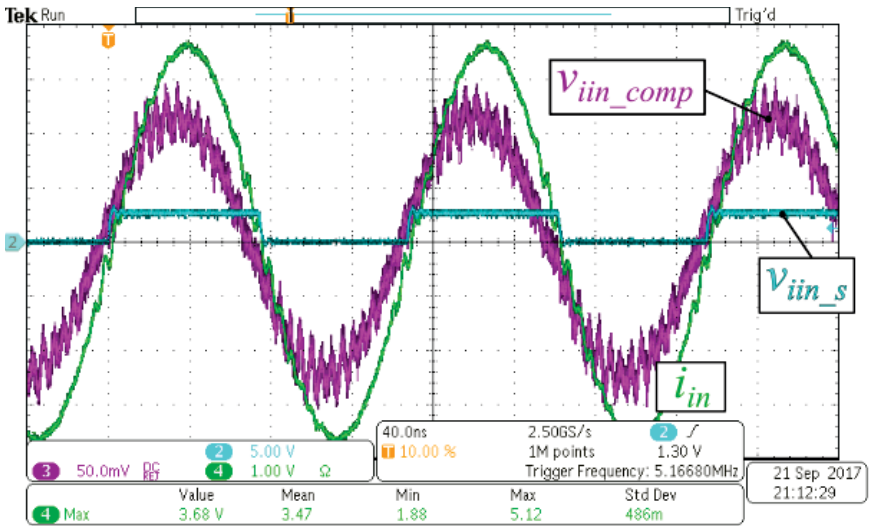


Figure 5.4: Waveforms i_{in}, v_{iin_s}, and v_{iin_comp}. Waveform i_{in} is measured with a 50 Ω terminated current-sense transformer and consequently has scale units of voltage. The conversion ratio is 1 V to every 0.2 A.

This current sensing system works well, but it is not without flaw. Creating a transformer for current sensing at 6.78 MHz is a non-trivial task in regards to parasitic capacitance. The parasitic capacitance from the primary winding to the secondary winding proved itself relevant during design. Common mode current uses this parasitic capacitor as a path to traverse from the switch nodes to ground through the filter network. Intelligent circuit placement and a grounded shield are used to reduce the negative impact of common mode current on the sensing network. The shield effectively provides a common mode path to ground, allowing the unwanted current to circumvent the sensing network. By these methods, presence of common mode current is significantly reduced, but not completely removed. A picture of the shield (covered in blue electrical tape for insulation) can be seen in Figure 5.5.

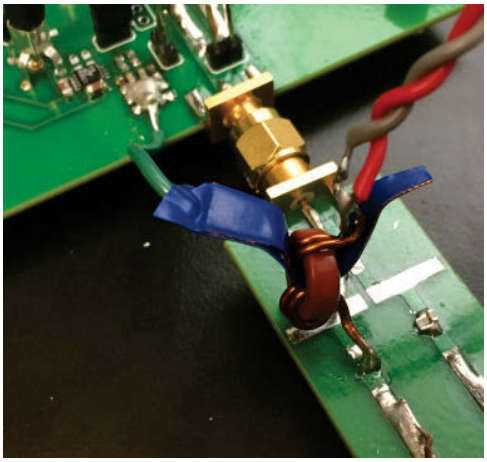


Figure 5.5: Shielded current sense transformer.

The sensing network also demonstrates imperfect behavior at low current levels. Figure 5.4 shows the signal at the comparator nodes, v_{iin_comp}. Although it fundamentally acts as expected, there is a substantial amount of noise coupled onto it. One can imagine that as the fundamental component decreases that signal will be dominated by noise. This is the case for small input current levels, and the result is a noisy sensing signal. Figure 5.6 shows the distorted output signal v_{iin_s} when i_{in} is small.

The voltage and current sensing signals are transmitted to an FPGA where they are used to control the rectifier's input phase angle. Given the circuit model presented in the previous chapter, it is possible for the FPGA to regulate phase with the current sensing signal alone. This is done by accounting for the relationship between α and ϕ within the FPGA code. However, using both voltage and current sensing enables the FPGA to utilize feedback until the required phase is achieved. In either operating

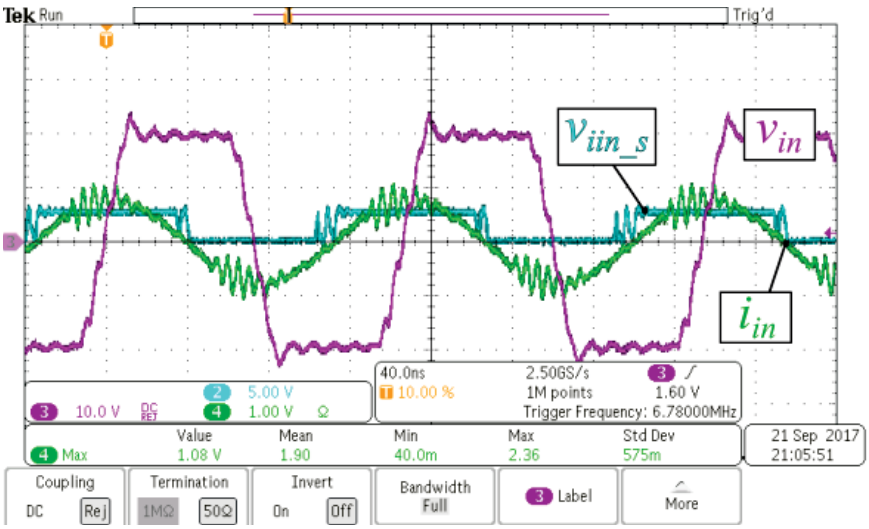


Figure 5.6: Distortion of v_{iin_s} at low current levels due to noise in v_{iin_comp} signal.

scheme the current sensing is critical, and it is for this reason that the current sensing scheme is presented here in detail.

5.2 FPGA and Loop Set-Up

The controller used in this work is DE0-Nano system, built around an Altera Cyclone IV EP4CE22F17C6N FPGA (the FPGA named in chapter 4). The gate driver input signals are supplied by the Altera FPGA, and the current sensing square wave is supplied to the FPGA. The FPGA uses this signal to control the timing of the switching action relative to the input current.

The experimental setup is altered due to the incorporation of sensing. The reference signal from the second function generator is no longer needed because it is replaced with the current sensor. Consequently, the experimental layout changes from what Figure 4.1 depicts. The experimental setup realized by the techniques

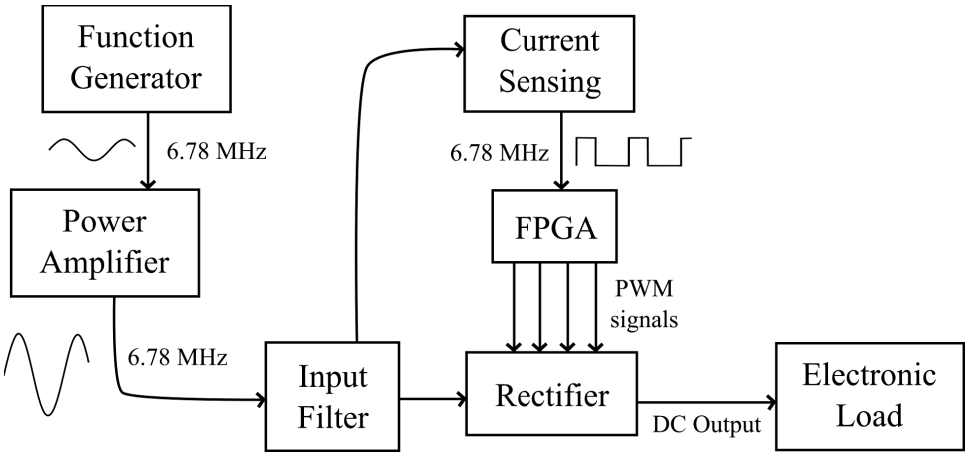


Figure 5.7: Basic closed loop configuration.

discussed in this chapter is shown in Figure 5.7. Note the presence of the current sensor that replaces the second function generator.

If the synchronous rectifier were implemented in an entire WPT system, the FPGA would regulate the variables α and t_d such that ZVS is achieved for the desired input phase ϕ, a value likely assigned at the system-level. In a real implementation the required value of ϕ is likely a function of the most efficient loading condition for the entire system, as the rectifier input angle affects the efficiency of the rectifier, coils, and inverter. The tests shown in this thesis do not include an entire WPT system and are consequently only demonstrating the rectifier's ability to regulate α and t_d and inadvertently ϕ and the ZVS, ensuring that the rectifier could operate in a full WPT system.

5.2.1 High Frequency Clock

The DE0-Nano board has an on-board 50 MHz clock, and using a phase lock loop (PLL), the 50 MHz is boosted to a stable 244 MHz high frequency clock signal. This frequency is chosen because it is almost an exact even multiple of 6.78 MHz, which means that there are 35.988 "sub-clock" periods within a single 6.78 MHz clock period. An even number is convenient because it allows for symmetrical half periods, i.e. Q_1 and Q_4 "ON" for 14 clocks, a 4 clock dead time, Q_2 and Q_3 "ON" for 14 clocks, and another 4 clock dead time. If the high frequency clock is an odd multiple, 35 for instance, the per-period clock distribution might be something like 14-4-14-3 instead of 14-4-14-4. This lack of balance is non-ideal and should be avoided as it causes circuit asymmetry.

The period of 6.78 MHz is 147.49 ns long. In the case of a 244 MHz, the clock period is 4.098 ns, making the discrete step size of the sub-clocks within one 6.78 MHz period 2.78% of the period. In terms of phase, this means that the resolution achieved is 10°. Therefore, given a control clock frequency of 244 MHz, varying the PWM signals by one clock edge results in a 10° change in the value of α. A higher resolution requires a faster clock speed. While the DE0-Nano has PLL functionality capable of generating clocks greater than 300 MHz, testing with clock frequencies above 244 MHz produced unstable results.

For these reasons, the 244 MHz clock is used in this research. This frequency delivers the highest stable-operation, even-multiple sub-clock resolution given the

current testing system. It is possible to improve system resolution with more complex processors and/or techniques, but for the focuses of this work, the aforementioned resolution is sufficient for demonstration the functionality of the proposed circuit.

5.2.2 Frequency Checking

The fundamental frequency of the system is also the switching frequency of the rectifier. As such, the rectifier's switching frequency is determined by the power source. During experimentation, a power amplifier supplies the input signals, and in a real application, an inverter and coupled WPT coils provide the input power. In either case the switching frequency is set by a mechanism external to the rectifier. Because the filters, thermal design, and auxiliary control components are designed specifically for 6.78 MHz operation, the accuracy of the input frequency is critical.

Input frequencies significantly higher than 6.78 MHz make circuit parasitic elements more relevant and switching-related losses larger. Each of these characteristics could easily damage the circuit in a variety of ways. Furthermore, the circuit sensing schemes are not verified for higher frequency operation. Especially due to the rectifier's emphasis on input phase, assuming that the sensing schemes will work with precision at frequencies above 6.78 MHz is ill advised. Again, parasitic elements and frequency-dependent impedances cause behavioral change for the sensing circuitry as the fundamental grows above 6.78 MHz, not to mention that IC component delay becomes more significant.

Frequencies lower than 6.78 MHz also pose a potential problem. First, the filtering elements will be tuned to the wrong frequency. This affects both the resonant WPT input filter (coil and resonant capacitor) and the output capacitance, which is assumed to be large enough to remove significant ripple. In the case that the input frequency is too low, the output ripple will not be sufficiently mitigated, causing a significantly large double frequency component at the output. Furthermore, the Qi Standard for WPT exists at frequencies in the 100 kHz range, and coupling to one of these systems by accident is not desired.

For all of these reasons, it is important to verify the frequency of the input power signals. The FPGA is capable of doing this task using the input current sensor and the 244 MHz clock. When an input current is detected, the FPGA counts the number of 244 MHz clock edges during one period. This allows the FPGA to derive the frequency of the input signal, given a level of potential error. The error occurs due to the offset of the edge trigger time of the input current sensing signal relative to the 244 MHz signal. This error is ± 2 sub-clock periods, or $\pm \sim 8$ ns. To account for small measurement error in the system, the required sub-clock edges measured within a period is set to 36 ± 4. Practically, frequencies below or above 6.78 MHz by a few megahertz or more will disallow the FPGA to send PWM gate signals.

5.2.3 PWM Generation

Once a PLL is used to successfully create a stable 244 MHz clock and the system input frequency is verified, the FPGA is equipped to regulate the rectifier's gate switching

signals. The sub-clock edges are counted during each 6.78 MHz period by a variable $gCount$. Each switch is assigned a variable of type integer signifying the end of the dead time and a variable of type integer signifying the end of the on time. For switch 1 these variables are $pass1dt$ and $pass1Ton$ respectively. Given the control scheme used in this work, Q_1 and Q_4 will always be in the same state, as will Q_2 and Q_3. For this reason, the variable parameters for these switch pairs will always be the same. For example, $pass1dt$ and $pass4dt$ will be equal, as will $pass2Ton$ and $pass3Ton$.

The code is written such that no two intervals can be active together. This is important because a malfunction in the switching intervals could translate to unproductive or potentially dangerous circuit behavior. For instance, accidentally substituting the dead time interval II for conduction intervals I and III is unproductive. In this case, the switches never turn "ON," reverse conduction occurs through the GaN devices, and the rectifier acts as a poorly designed passive rectifier. Similarly, mistakenly turning on intervals I and III at the same time results in a shunt path, shorting both the input source and the output capacitance. A mistake of this nature likely causes catastrophic current levels.

Figure 5.8 shows the current sensing signal, 244 MHz clock signal, and the output PWM signal V_{gs1}. For simplicity, the constant propagation delay between the PWM signal V_{gs1} and input voltage v_{in} is not shown. Furthermore, the zero-crossing of i_{in} and the sensor output are supposed to occur at the same instant in Figure 5.8. Comparisons of the variable $gCount$ to both $pass1dt$ and $pass1Ton$ are used to create

the PWM signal V_{gs1}. Recall that $V_{gs1} = V_{gs4}$, thus the rising and falling edges of signal V_{gs1} mark the beginning of intervals I and II, respectively.

This type of control scheme allows for V_{gs1} - V_{gs4} to be shifted in time relative to the input current sensing signal and consequently the input current itself, i_{in}. This time shift results in a change of the α (the angle between the zero-crossing of i_{in} and the middle of the dead time, t_d). Recall from Section 5.2.1 that the step changes in α are sized relative to the frequency of the sub-clock and are $\sim 10^{\circ}$ for a 244 MHz sub-clock frequency.

To implement this functionality, the variable $gCount$ is synchronized with the i_{in} sensing signal. That is, the first 244 MHz clock edge after the i_{in} sensing signal always denotes $gCount = 1$. In this way, $gCount$ is anchored to the sensing signal, and each 6.78 MHz period of sensed i_{in} is counted from 1 to $\sim$36. With $gCount$ defined in this manner, the PWM signal V_{gs1} shifts relative to i_{in} when $pass1Ton$ and $pass1dt$ are edited. The same shift is achieved for PWM signals V_{gs2} - V_{gs4} by changing the appropriate variables. Figure 5.9 illustrates almost the same thing as Figure 5.8, but the change of variables $pass1Ton$ and $pass1dt$ results in a different phase between i_{in} and v_{in}.

This control scheme creates a good code environment for dynamically changing the input phase of the rectifier. As shown by the combination of Figures 5.8 and 5.9, the control scheme allows α to be either positive or negative, equipping the rectifier to generate both inductive and capacitive equivalent loads. This capability is important in that it enables the system to better address dynamic WPT loading conditions.

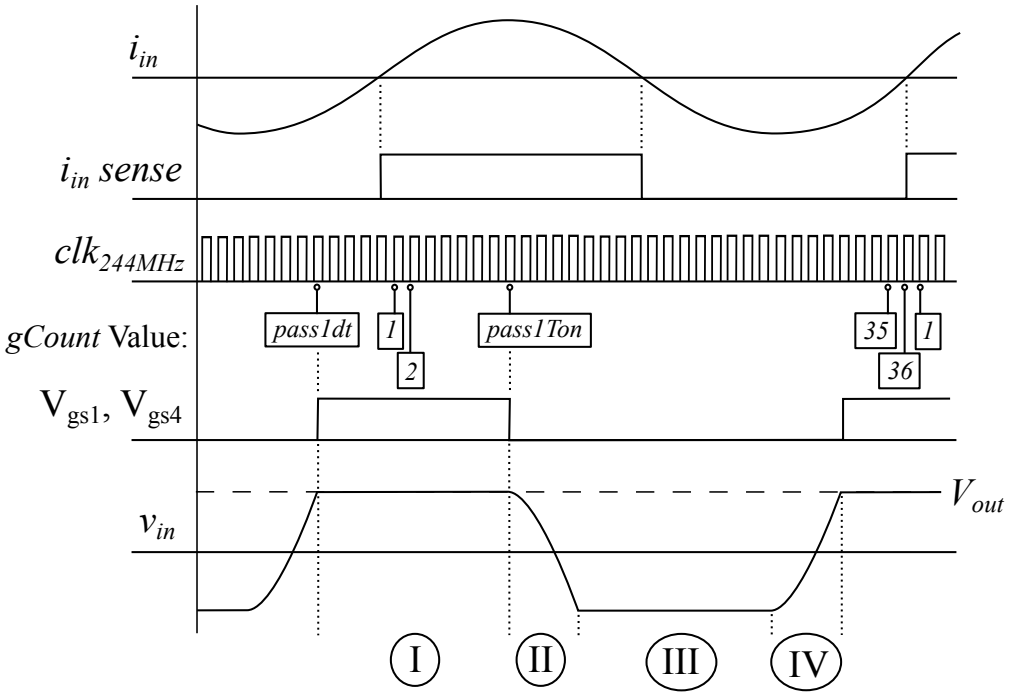


Figure 5.8: Sensing, clock, and PWM signals as generated relative to the circuit signals i_{in} and v_{in}.

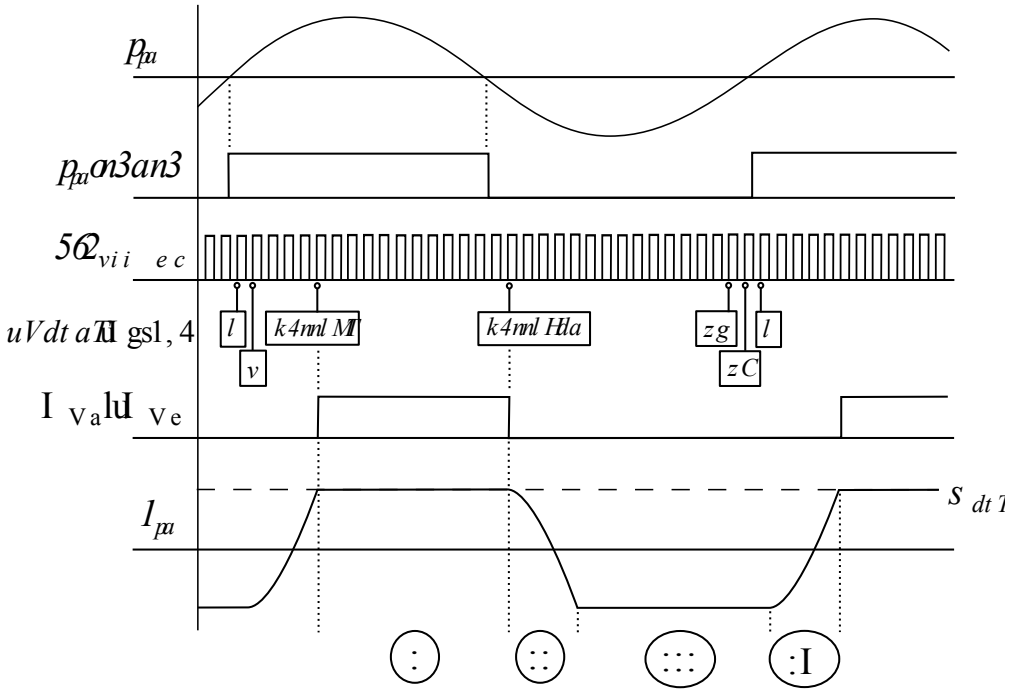


Figure 5.9: Sensing, clock, and PWM signals as generated relative to the circuit signals i_{in} and v_{in} with a positive phase shift ($+\alpha$).

5.2.4 Frequency Synchronization

In a generic DC-DC converter, take the buck converter for example, the switching frequency is assigned by the designer. For a given topology or design, the frequency may change with operating point, but overall, a converter's switching frequency is a control variable. This is not true for rectifying networks. A diode bridge switches at a frequency dictated by the input waveforms, and a synchronous network must do the same. This is potentially difficult for a synchronous network, however, and it is especially difficult for a rectifier without a clock connection to the system supplying the input signals, as is the case with a WPT rectifier. This is the fundamental reason why the input power signals must drive the switching action – frequency synchronization.

A slight misalignment between the input frequency and the average switching frequency causes failed functionality, potentially resulting in reverse power flow, hard switching, and many other issues. As an example, if the synchronous rectifier switches at 6.780001 MHz while the input power signals have a frequency of 6.78 MHz, then that difference of 1 Hz means that the rectifier's switching signals will incorrectly traverse one period of the input signal every second. Initially, the desired α is correct, but during every other instance for the next second, the rectifier has an incorrect value for α. The same process takes place during the next second.

It seems a simple fix that 6.78 MHz is the required frequency for the system, but unfortunately this is not so. Designing an inverter and rectifier to operate at the same

frequency does not ensure that this problem will be avoided. It almost certainly will still be an issue due to the small non-idealities with clock systems. Each oscillator or clock circuit has some error. For devices like electronic watches this is relatively inconsequential. The clock error will cause a time skew of a few seconds or minutes over the course of the watch's lifetime, a small inaccuracy.

To address this difficulty, an average frequency is used. Recall that the sub-clock frequency is 244 MHz because it contains ∼36 periods within one 6.78 MHz period. The precise number of sub-clock periods is 35.9882. In practice, this means that 98.82% of the periods generated by the FPGA code contain 36 sub-clock rising edges, and 1.18% of the periods contain 35 sub-clock rising edges. The result is an average switching frequency that perfectly matches the input frequency. If the input frequency is slightly higher or lower, or if the sub-clock frequency deviates some small amount, the effective rectifier frequency adjusts accordingly. It adjusts because ratio of 35 to 36 sub-clock length periods is not directly controlled by the FPGA by means of a variable or algorithm. Rather, the control is somewhat organic, resulting from allowing the phase relationship between the sensing signal and 244 MHz clock to be arbitrary and changing.

Figure 5.10 shows how the number of sub-clock edges can change within one period of the fundamental. In Figure 5.10a a sub-clock rising edge happens just before the start of the period, resulting in what would be the 36th sub-clock edge being pushed after the next rising edge of v_{iin_s}. In Figure 5.10b a sub-clock rising edge occurs just after the start of the v_{iin_s} period, resulting in a total of 36 sub-clock edges within on

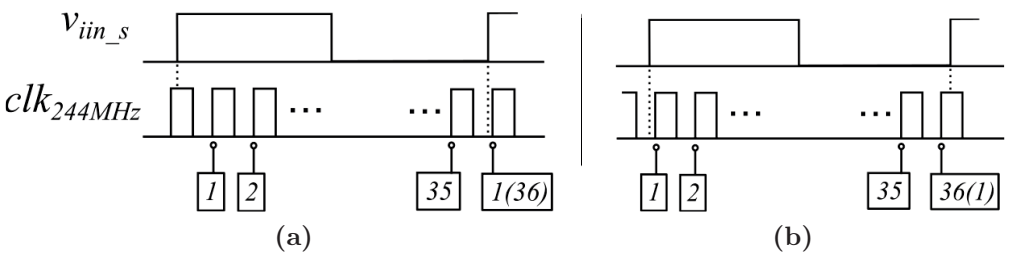


Figure 5.10: Number of 244 MHz sub-clock signal edges changing from (a) 35 to (b) 36 as the alignment of the sub-clock shifts with respect to the rising edge of v_{iin_s}.

fundamental period. As the relationship between these two signals is unconstrained by design, the resulting average sub-clock rising edge count converges to the precise number of 244 MHz periods needed to match the input frequency. Again, in an ideal case that number is 35.9882, meaning that 98.82% of the fundamental periods use 36 sub-clock edges for generating control PWM signals.

5.3 Experimental Closed Loop Operation

The system is first verified for a single control phase, α, and dead time, t_d. The value of t_d is preassigned in terms of sub-clock edges in the FPGA for a near perfect ZVS transition for the operating point under test. The sensing provides a reference signal, PWM signals are generated, and regulation of the input signals i_{in} and v_{in} is attained according to the programmed value of α. Confirming basic functionality in this way is necessary, but a rectifier used in a real system is expected to change both α and t_d dynamically to optimize the entire WPT system.

For this reason, additional functionality is added to the closed loop testing. The code is updated to include switch action of a physical push button. The push button

is located on the FPGA and is debounced as a feature of the DE0-Nano board. Upon pressing the button, the FPGA code updates the variables responsible for controlling both α and t_d. With this system, the rectifier input phase is changed without rewriting and recompiling code, better mimicking the behavior of an actual implementation. Figure 5.11 shows waveforms acquired via the described system without recompiling code or turning off power to the circuit. A button press occurs between each pair of waveforms, gradually changing the phase relationship between v_{in} and i_{in}. The value of α is changed by one 244 MHz period with each button press, thus Figure 5.11 shows how the discrete steps in α translate to discrete steps in ϕ.

The value of peak value of the input current (I_{in}) changes with each input phase because the amplifier's equivalent load is changing. For tests with a constant i_{in}, the gain nob on the power amplifier allows the engineer to regulate a constant I_{in}. Here, I_{in} is allowed to change because the capability being showcased is the rectifier's ability to edit its equivalent input phase with nothing but a button press.

Notice the "jitter" of waveform v_{in} at larger values of ϕ in Figure 5.11. This is how the varying number of sub-clock edges per period manifests on the oscilloscope screen. The oscilloscope has a hold functionality, meaning that multiple periods of the signal being measured are displayed at once. The jitter is made up of distinct lines and not a "blur." Each line in the jitter is a different number of sub-clocks edges within a period, and when all the periods (of different sub-clock edge counts) are overlaid using the same trigger edge, the end result looks like the v_{in} jitter seen in Figure 5.11.

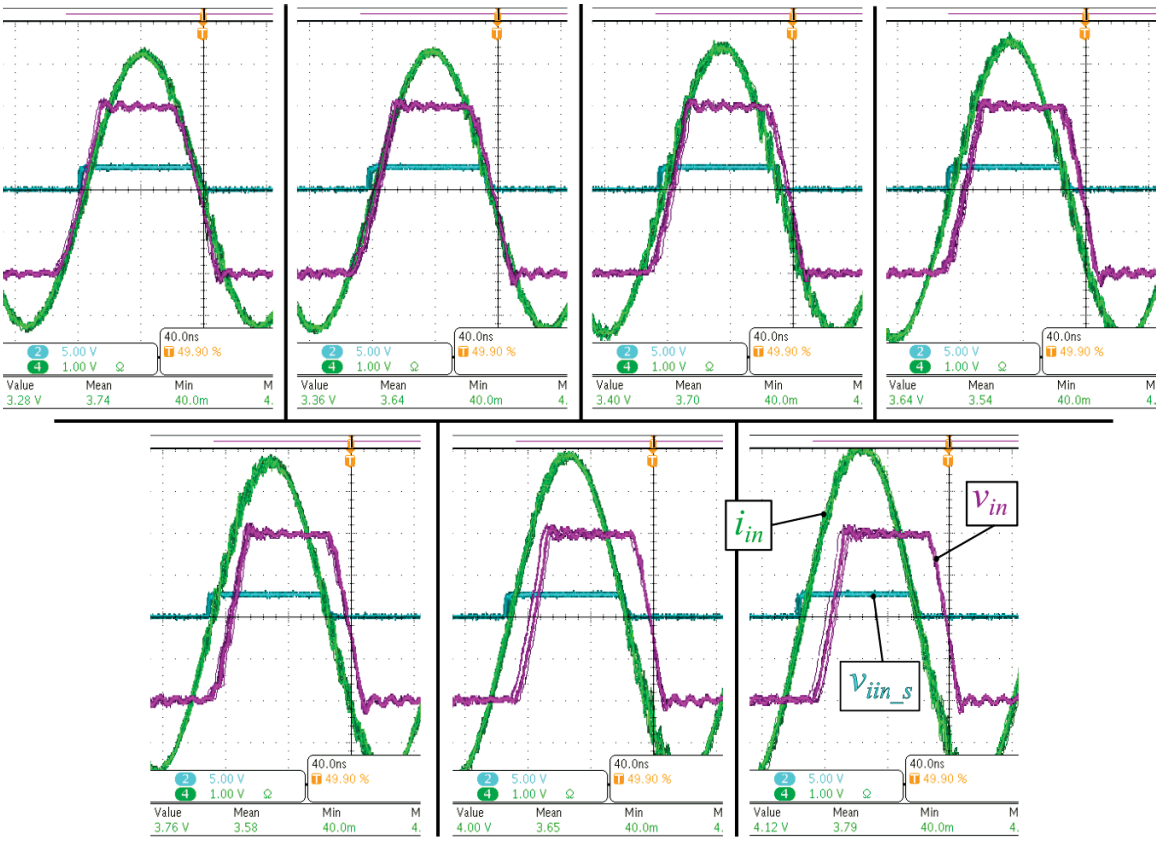


Figure 5.11: Waveforms v_{in}, i_{in}, and v_{iin_s} achieved via closed loop regulation with different values of ϕ cycled via a physical button press.

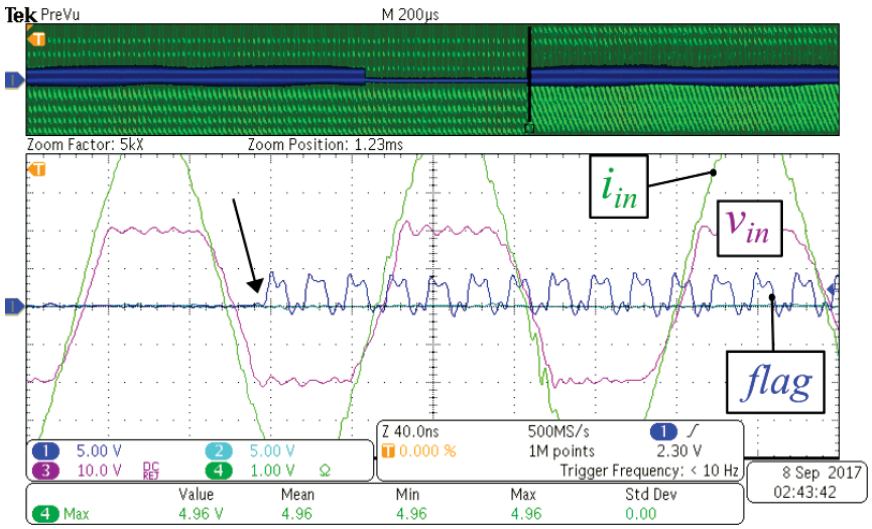


Figure 5.12: Transient condition with "flag" signal describing when button is pressed and α changed.

The transient characteristic while changing from one value of α to another is explored as well. The assumption herein is that the steps in α are small, and in this case that means stepping by one sub-clock edge at a time. The precise value of t_d changes with every new value of α, but t_d in terms of discrete sub-clock periods changes with only certain transitions in α. In either case (t_d changing or not), the FPGA code is designed for continued gate signal generation given a change in α. There is no pause in rectifier operation as input phase is changed.

Figure 5.12 captures the transient condition of the button press functionality showcased in Figure 5.11. The signal named "flag" is a FPGA pin set LOW when the button is untouched and set to the 50 MHz internal clock when the button is depressed. Therefore, the arrow on Figure 5.12 indicates the instance when the button is pressed and the value of α updated. During this transient, the rectifier does not stop regulating, and the input signals do not distort. There is a noticeable difference

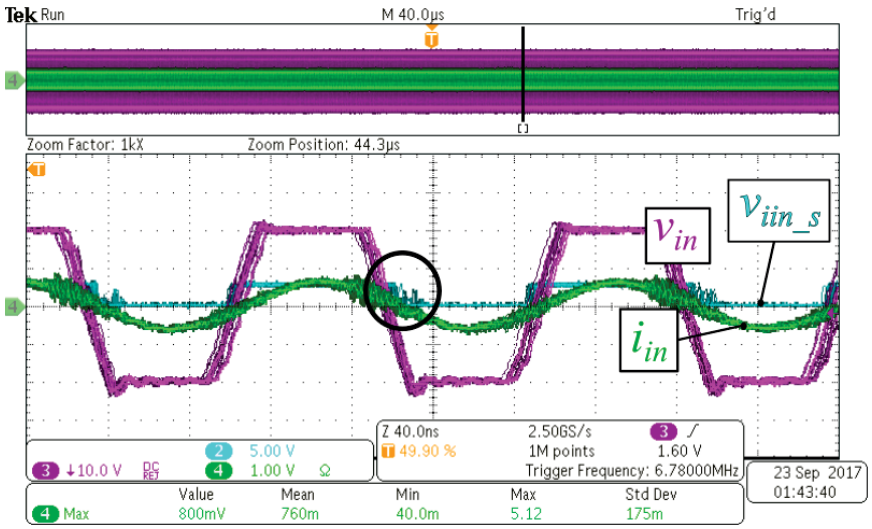


Figure 5.13: Closed loop regulation with sub 1 W output power via filtering of sensing signal v_{iin_s}.

between the v_{in} dead time transitions before and after the button press. The cycles after the button press are generated using updated values of $pass1dt$, $pass1Ton$, $pass2dt$, etc. Thereafter, the circuit waveforms (i_{in}, v_{in}, i_L, etc.) gradually approach a new steady state operating point.

Having $gCount$ constantly locked onto the current sensing signal, v_{iin_s}, makes transient operation much easier to handle. Recall that the PWM signal V_{gs1} is generated by comparing $pass1dt$ and $pass1Ton$ to $gCount$. Therefore, in order to change α either $gCount$ or $pass1dt$ and $pass1Ton$ must change. The chosen implementation allows for t_d and α to change dynamically in the middle of a period (when $gCount \neq 1$) instead of having to introduce a step change in the value of $gCount$ and potentially generating incorrect PWM signals during the transition period.

Finally, low power operation is tested with the closed loop setup. Any noise on i_{in} translates to noise on v_{iin_s}, a signal used to generate the gate signals. At low power levels the noise begins to dominate i_{in}, making low power operation difficult to achieve in the closed loop scheme. In spite of this, the output power of the test point shown in Figure 5.13 is around 0.8 W. Furthermore, the circled region in Figure 5.13 shows v_{iin_s} distorting due to noise on i_{in}. If the value of $gCount$ is set to 1 on each rising edge of v_{iin_s} as previously described, then it is expected that $gCount$ resets in the middle of the period because of such noise.

The solution strategy is simple but effective. A second criteria is added to the reset scenario of $gCount$ such that it cannot be set to 1 until it is *at least* of value 32. Furthermore, the rising edges of v_{iin_s} are considered illegitimate unless $gCount$ is above 32. This is valuable because v_{iin_s} is used in other parts of the FPGA code. This method effectively creates a co-dependency between $gCount$ and v_{iin_s} wherein neither can be triggered until the latter portion of the period. Overall, elegant code solutions like this expand the capability of the circuit sensing, and in this case, enable closed loop operation at much lower powers.

5.4 Summary

The input current sensing strategy and topology is described and explained. The closed loop experimental setup is shown, noting how current sensing is used to complete the loop. The FPGA code includes a high frequency clock, input frequency

verification, PWM generation, and input power frequency synchronization. Closed loop experiments show the rectifier's input phase changing according to the FPGA control mechanisms. Transient conditions are shown to be stable and fast with respect to the fundamental period, and when sensing at low power, noise is shown to be well handled by the FPGA code architecture.

Chapter 6

Conclusions and Future Work

6.1 Overview

6.1.1 Challenges in WPT

Magnetic resonant wireless power transfer employs a circuit resonance tuned to the fundamental frequency. The PTU and PRU are loosely coupled, allowing devices more placement freedom relative to the transmission source. The AirFuel Resonant standard for WPT operates at a fundamental frequency of 6.78 MHz. This frequency is much higher than inductive WPT standards that generally operate in the 100's of kHz range. While operating at a higher frequency equips the standard to accomplish things like improved circuit compactness, longer transmission distance, and a higher degree of misalignment forgiveness, the increase in frequency also bring other issues

to relevancy. Things like parasitic circuit elements, switching time and loss, and harmonic distortion become more prominent factors in design.

The coils of WPT systems cannot be shielded due to their need to couple onto magnetic fields external to their respective devices. Unfiltered harmonic distortion across a WPT coil results in radiated EMI relative to the levels of distortion. For this reason, it is common to include multistage filters in circuit design to mitigate the EMI that occurs outside ISM bands. In order to reduce the need for filtering, low THD circuits like the Class E rectifier are proposed in the literature.

Magnetic resonant WPT sees a wide range of loading conditions due to the increased device placement freedom, ability to host multiple PRUs, cross-coupling, and various PRU power levels. Such dynamic loading parameters cause efficiency problems when operation falls outside of the most optimized design space. Design wherein all loading conditions are considered has been shown to be valid, and real-time response to dynamic loading via synchronous rectification has been done. However, at 6.78 MHz the hard-switching involved in synchronous rectification proves to have too much loss for operation.

The proposed GaN-based synchronous rectifier addresses these issues by elegant use of a resonant tank. The tank creates elongated ZVS transitions that serve to drastically reduce switching loss while simultaneously lowering harmonic distortion. Furthermore, with proper design, the rectifier is able to achieve control of its input phase, thereby equipping the WPT system to respond to the wide range of loading conditions.

6.1.2 Modeling and Design

Fundamentally, the synchronous rectifier controls Q_{1-4} such that the input current, i_{in}, is rectified to a DC output. i_{in} is supposed to be an ideal current source, and the timing of the switching action is set by the variables α and t_d. A precise derivation of the dead time improves modeling accuracy. MATLAB is used to compare the precise model to a linear model, illustrating that the improved precision is necessary for accurate design.

L_r and C_r are design parameters whose value is contingent upon input power, THD requirement, efficiency requirement, and phase control range needed. Given a test point, the resonant tank elements are swept to quantify the $L-r$ and C_r design space. It is shown that some designs are poor designs that deliver far too much or far too little resonant tank current. Two example designs are shown to illustrate the designer's choices in efficiency verses THD verses phase control.

6.1.3 Open Loop Experimental Verification

The practical PCB design points of gate driver choice and parasitics are analyzed. The LM5114 gate driver is used in lieu of the LM5113 half bridge driver due to the lossy reverse recovery mechanism inherent to the internal bootstrap diode of the LM5113. PCB parasitic inductances are reduced by tightening the layout of both half bridges and the resonant tank. Using the improved PCB design, the open loop experiment is described and shown. Testing includes the use of two synchronized function generators

and a power amplifier. Test points are taken and overlaid onto model data, and it is shown that parameter trends like THD and P_{in} are well-represented by the model.

The experimental data is shown to diverge from the model at low output power levels. An investigation considering two current probes, each with bandwidth well above the fundamental, reveals that skew is a significant factor in measurement value. The validity of the experimental data (power measurements calculated from experimental waveforms) is then evaluated with a thermal imaging camera. The results more closely agree with the model, implying that circuit losses are not as high as measured in the experiment. A case is made that low power, high frequency, non-sinusoidal waveforms are difficult to measure with a high degree of precision.

6.1.4 Closed Loop Operation

Input voltage sensing is established, and input current sensing is evaluated. A current sensing scheme is designed to step down voltage levels, filter noise, and provide a corrective phase shift. The sensing scheme is implemented, and when combined with comparator delay and parasitic elements, provides a well-aligned sensing square wave, v_{iin_s}.

The closed loop experimental setup is shown and discussed. The setup mirrors that of open loop except that one of the function generators is replaced with the signal v_{iin_s} and the FPGA code updated. Mechanisms of the closed loop code are described. These include the 244 MHz sub-clock, input frequency verification,

the PWM generation system using variables like $gCount$ and $pass1dt$, and precise frequency synchronization via differing sub-clock edges within a period.

Experimental waveforms are shown to showcase the system's capability to change input phase without reprogramming the FPGA. A transient condition is pictured, and the code structure is said to complement phase change, allowing for continuous operation during the time when the step change in phase causes circuit waveforms to have to re-converge to steady state. Finally, the system is able to operate at sub-watt power levels due to an FPGA code codependency between the variable $gCount$ and the input signal v_{iin_s}. This acts as a filter for input current noise and the consequent distortion on v_{iin_s}.

6.2 Conclusions

Wireless power transfer is increasing in popularity. As wireless data transfer did years ago, WPT will revolutionize the industry once the technology is user-friendly enough for widespread adoption. Currently, challenges with the current state of the art deter such user-friendliness, and the circuit proposed in this thesis addresses these challenges.

This thesis presents the GaN-based synchronous rectifier with reduced THD and input phase control as a good candidate for 6.78 MHz wireless power transfer. It is shown that the introduction of a ZVS resonant tank mitigates switching loss to such a degree that high efficiency synchronous rectification is possible at 6.78 MHz. That

same ZVS tank, by proper design, enables the rectifier to lower harmonic distortion at the input, thereby reducing the need for filtering the signals before the secondary coil. It is also shown that the low THD ZVS tank can be designed to account for a system's required input phase control range. Because of this, the rectifier is able to control its load angle dynamically, adjusting for a wide range of WPT system loading conditions in real time.

These improvements do not come without cost, and the disadvantages of the proposed circuit should also be named. First, switch control adds both complexity and volume. In this work, the switching losses are assumed small and ignored, and the space taken up by switch control elements is not considered because no attempt at miniaturization is made. If mass-produced, the gate driver circuitry and FPGA would likely be consolidated into a single integrated circuit chip. Although an IC is small, a switching circuit will always have control overhead in terms of both loss and space. Compared to passive solutions like diode full-bridges and diode Class E rectifiers, this must be considered.

Sensing circuitry can also be considered a disadvantage. As discussed in chapter 5, accurate and precise zero-crossing sensing is non-trivial at 6.78 MHz. Again, no significant attempts were made in this work to miniaturize the sensing schemes, but even if the sensors are optimized for size, they still take up some space that is potentially not necessary in other circuits. Compared to passive solutions, this is added complexity, space, and loss.

6.3 Future Work

Lastly, this project contains areas that either require more work or invite more work. Those areas that require more work do so because a portion of the system is unfinished or only partially modeled. Those areas that invite more work seem promising in terms of improved design or significant finding for the field of resonant WPT.

6.3.1 Model Improvement: Input Voltage

When multiple receiving units couple onto a single transmitting coil, the equivalent load is like each of the PRUs connected in series. If the transmitter acts as a voltage source, then removing a PRU creates a step in the transient power delivered to all PRUs that remain coupled to the transmitter. For this reason, it is beneficial for the transmitter of a resonant wireless power transfer system to operate as a current source [48]. Also, one of the differentiating factors between IPT and WPT systems is that of coupling factor. In a resonant WPT system, the coupling factor is generally much lower than in an IPT system where it is assumed to be large. Figure 6.1 shows a resonant WPT system with a current source for the transmitter. The circuit in Figure 6.1 uses a T model for the primary to secondary transformer and includes the coupling factor, k, which is determined by the quantity of shared magnetic field between the WPT coils. The capacitor C_{WPT} is added to created a resonant filter with $(1-k)L_s$ tuned at the fundamental.

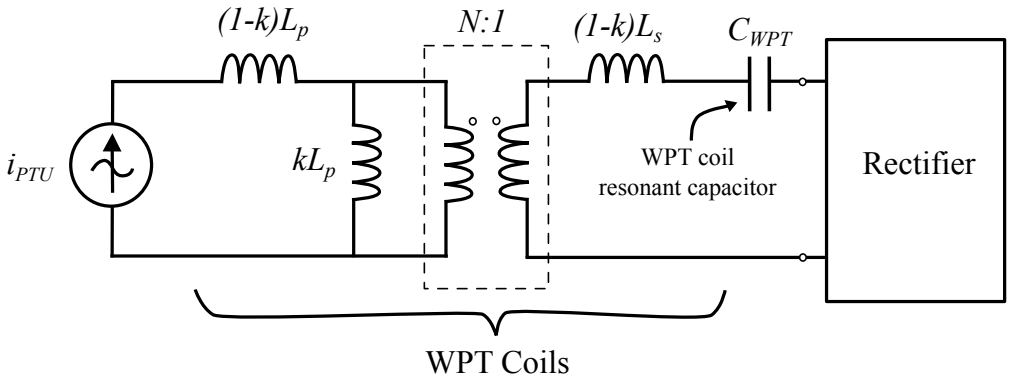


Figure 6.1: WPT system model with a current source PTU and the coupling factor included in the transformer model.

The primary side input current, i_{PTU}, is split between the branch with impedance kL_p and the ideal transformer. When the coupling factor is considered small kL_p becomes small and carries the majority of i_{PTU}. Shown in Figure 6.2a, the model presented in this paper is built around an ideal current source, i_{in}, at the input of the rectifier. However, because most of the current i_{PTU} flows through magnetizing inductance kL_p, a step change in load does not drastically change the current in this branch. Therefore, the voltage across kL_p, and consequently the voltage across the receiver windings, stays relatively constant as well. For this reason, it is more accurate to model the proposed circuit as shown in Figure 6.2b.

If i_{PTU} is an ideal current source, then this difference in the model does not particularly matter for steady state operation. A voltage containing only the fundamental component will traverse to the secondary side, and that voltage will generate a sinusoidal input current for the rectifier. This, of course, can be modeled as an ideal input current. However, the difference in modeling technique becomes relevant when looking at a transient condition during a change of state or when the

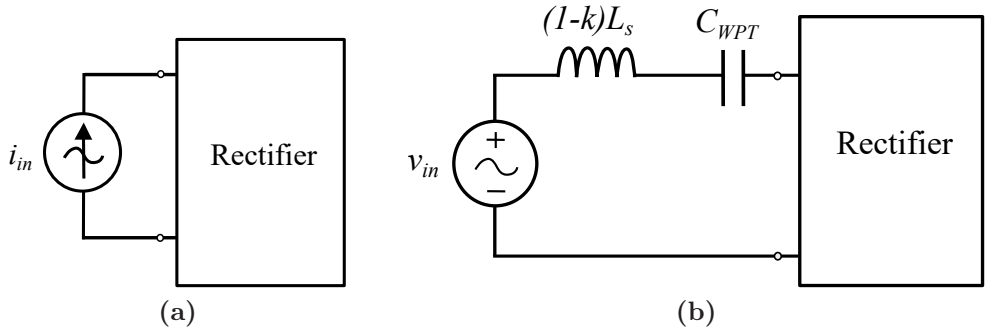


Figure 6.2: Diagrams of the (a) current model built with an input current source and (b) suggested model accounting for the low coupling coefficient.

magnetic field contains harmonic content (i_{PTU} is not ideal). During a transient condition, the circuit will respond differently if driven by a voltage source than it will if driven by a current source. If there is distortion in the magnetic field, then the secondary side input voltage has some level of THD. In this case, the quality of the filtering elements $(1-k)L_s$ and C_{WPT} becomes a factor.

As stated in chapter 4, the circuit is supplied by a power amplifier, which acts like a voltage source. In the experiments, an inductor and capacitor are added in series with the rectifier to simulate $(1-k)L_s$ and C_{WPT}. In this way, the experiment is set up much like Figure 6.2b. Insofar as the quality factor of the filter is high, the model in Figure 6.2a is sufficient (in steady state). In order to maintain the model's applicability when using an input current source to model the rectifier, one must take care that the values of the filter elements used in experimentation are both practically realistic and capable of adequate filtering. A filter with an inductance value that is too low will fail to attenuate non-idealities, rendering the model in Figure 6.2a inapplicable due to harmonic distortion on i_{in}. A filter with an inductance value that

is too high will experimentally match Figure 6.2a but will be impossible to implement in a real WPT coil design. The experimental results shown in chapter 5 find this balance, using inductor and capacitor values of 3.7 μH and 143 pF respectively.

The model presented in this thesis and shown in Figure 6.2a is usable given that the designer understands its limitations. A more accurate system model is given by Figure 6.2b. This improved model enables a designer to account for transient conditions more accurately, harmonic distortion at the input, and real circuit elements $(1-k)L_s$ and C_{WPT}. Because the rectifier is eventually going to be integrated into a WPT system, improving the model to account for real WPT circuit characteristics and transient conditions is beneficial.

6.3.2 Rectifier Control: Navigation of States

Chapter 5 demonstrates the rectifier regulating its own switching frequency and input phase. The next step in the control process is to establish the rectifier's choice of desired state. Here, the term 'state' refers to the circuit waveforms; a change in any one waveform propagates to affect all others and inherently defines a change in the rectifier's operating state. Assuming that the input and output are both at some arbitrary operating point, how does the rectifier decide on its control strategy? The experimental results shown in this theses are conducted with given values for V_{out} and I_{in}, making the derivation of α, t_d, and other circuit parameters possible. Future work should include finding a solution strategy for how the rectifier makes decisions about which operating states to choose and how to achieve them.

One thing is clear: something will need to be sensed. The current zero-crossing sensing is used to control input phase and switching frequency. Similarly, the input and/or output will need to be sensed with regard to voltage, current, and/or power. While arguments can be made for any sensing scheme, this section will focus on a sensing scheme that uses V_{out} and I_{out}. The assumption therein is that sensing DC output values will be much simpler and more reliable than sensing high frequency AC signals.

The rectifier chooses the value of α, and the values of V_{out} and I_{out} are sensed. Given these three values, the rest of the circuit parameters can be calculated. In other words, there is one unique set of values for the variables ϕ, I_{in}, V_{in}, and t_d given α, V_{out}, and I_{out}. Once system parameters are calculated, then control decisions can be made by the rectifier.

One way to approach to determining system parameters is to compute them beforehand and then upload the parameter values to the FPGA in large tables. The MATLAB model presented in chapter 3 is constructed such that I_{in}, V_{out}, and α are input parameters, and the rest of the parameters are derived from those three. Figure 6.3 shows an example of data from that system. The THD is given in terms of V_{out} and α where each "sheet" in the graph is a different sweep value of I_{in}.

The same process is carried out for variables like I_{out}, t_d, and ϕ. In this way, the "operating space" of a given design can be mapped. Parameters like the hard-switch

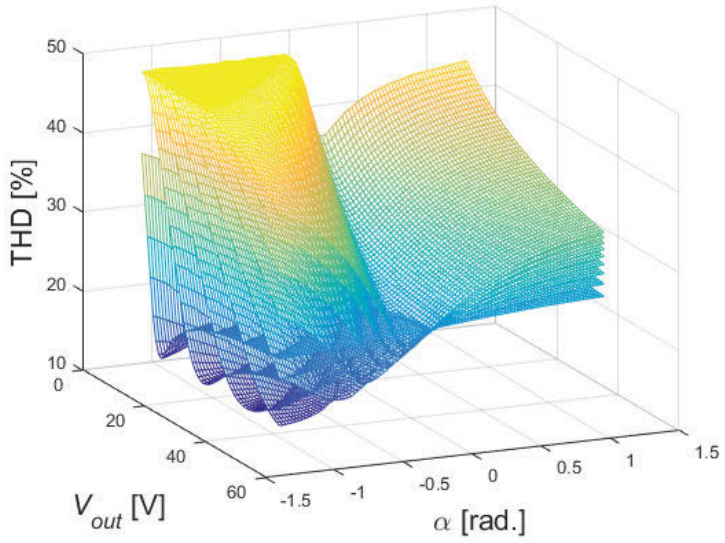


Figure 6.3: THD of a rectifier with $C_r = 1120$ pF and $L_r =$ nH as a function of V_{out} and α. Each of the different"sheets" is each a separate sweep of I_{in}.

and efficiency voltage are saved as well. Using the hard-switching voltage, all non-ZVS points can be filtered out of the data. Figure 6.4 shows the same THD data, all data points with hard switching greater than 2 V have been removed.

Given the sensing choice, it is more beneficial for the operating space to be mapped in terms of I_{out} instead of I_{in}. One way to accomplish this is to define n discrete steps between the minimum and maximum values of I_{out} within the design space. For each plane where V_{out} and α are constant, I_{out} and I_{in} can be interpolated to achieve a higher sampling resolution. The nearest match to each of the n values of I_{out} can be found and indexed. In this way, I_{in} can be described in terms of constant steps of I_{out}, and the indices can be saved and extended to all other circuit parameters such that those parameters are mapped in the same manner. Effectively, restructuring the data in this way makes I_{out}, V_{out}, and α the input parameters and I_{in} an output parameter,

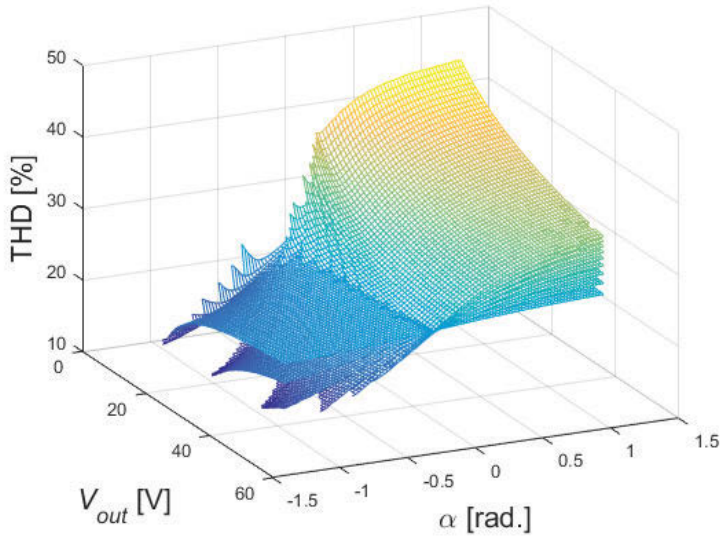


Figure 6.4: THD of a rectifier with C_r = 1120 pF and L_r = nH as a function of V_{out}, α, and I_{in}. Only the ZVS points are shown. .

matching the hardware sensing and control scheme. The goal of a manipulation of this type is visualized in Figure 6.5.

With the domain of the data shifted to match the known system variables, the data can be uploaded into the FPGA, or best fit equations can be used to characterize the operation space. The implementation of either of these is non-trivial. Data resolution and FPGA memory make the first option challenging and the inherent difficulty with curve fitting three dimensional data is a pitfall for the latter option. Realistically, a combination of the two techniques can be used. Equations should be used to characterize where either approximations can be made or the equations are reasonable, and discrete data of appropriate resolution can be utilized elsewhere.

However, none of this completely solves the problem of rectifier control. Given that all the data is available for the rectifier, there are still certain issues the circuit

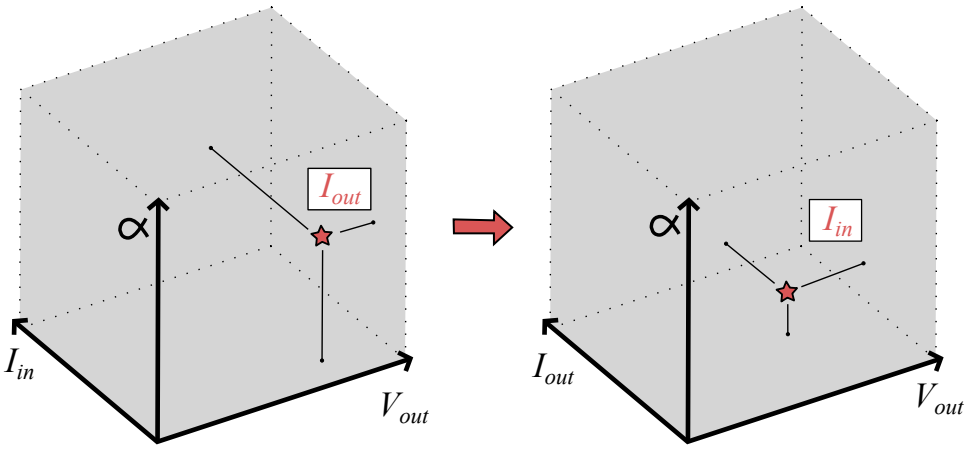


Figure 6.5: Illustration of data transformation from the $\{\alpha, V_{out}, I_{in}\}$ domain to the $\{\alpha, V_{out}, I_{out}\}$ domain.

is not capable of addressing. Namely, during a transient condition the rectifier may not be at a ZVS point. This is an issue because all of the data represented by Figure 6.5 is for perfect ZVS transitions. In this case, the system is at an unknown operating point, having no data or equation by which to characterize a hard-switched or diode-conducting circuit. How does the rectifier attempt to re-converge onto a ZVS operating point? Furthermore, how does the rectifier decide on the operating point upon which it attempts convergence? Assuming the operating space is characterized, these are essential control questions that must be addressed.

Perhaps the rectifier assumes ZVS at all points, monitors V_{out} and I_{out}, and chooses a value of α such that a system level constraint is met (lowest THD, required input phase, highest efficiency, etc.). If a non-ZVS point occurs with this system then the rectifier does not detect it. Instead, it uses the measurements available and adjusts α accordingly to the set goal. Upon adjusting α the sensing measurements change, and the rectifier adjusts again. Perhaps this technique allows waveforms to converge

to a ZVS state, perhaps not. Future work must consider schemes of this nature and evaluate the conditions under which the system will not be stable.

Another option is adding a sensing circuit to detect ZVS. In this case the rectifier is able to assume that any point of operation lies within the mapped operating space. It is also beneficial in terms of reliability and safety, creating a fail-safe for hard switching circumstances. The drawback is the additional size and complexity inherent to adding sensors.

Overall, there is a significant amount of work to be done on controlling the synchronous rectifier. The discussion presented in this section only serves to better illustrate the challenges of this control problem. There are plenty of options and techniques to evaluate, but each is a implementation detail in the larger problem statement: designing the rectifier to choose and navigate operating states.

6.3.3 Input Impedance Magnitude Control

As shown in Figure 1.3, a WPT system generally has a conversion stage between the rectifier and the battery. This DC-DC converter adjusts its equivalent resistance to regulate the battery charging process. This allows the system to regulate the battery's charging current at any point during the charge cycle.

As discussed in the literature review, it is possible for a synchronous rectifier to control both the magnitude and phase of its input impedance [34, 35]. Control of the magnitude of the input impedance is established by a duty cycle switching scheme. Switch pair Q_1 and Q_2 and switch pair Q_3 and Q_4 are turned on together, briefly

shorting the switch nodes. In each case, i_L is held constant, and the input voltage is zero. This allows the rectifier to establish a duty cycle defined as the ratio between the time the input is connected to $\pm V_{out}$ and the time the input is set to zero.

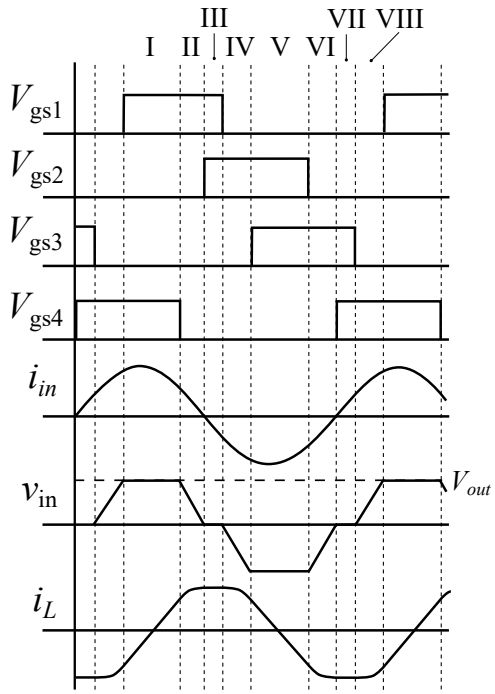


Figure 6.6: Idealized waveforms demonstrating operation of the synchronous rectifier with a duty cycle switching scheme.

Figure 6.6 shows a linearized approximation of how the switching scheme might work with resonant transitions. The duty cycle can be adjusted along with the input phase such that the rectifier is able to present any impedance within the range designed into the system. Derivation of system model and resonant tank design space are likely similar to the proposed rectifier but should be re-derived to for this switching scheme.

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Vita

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